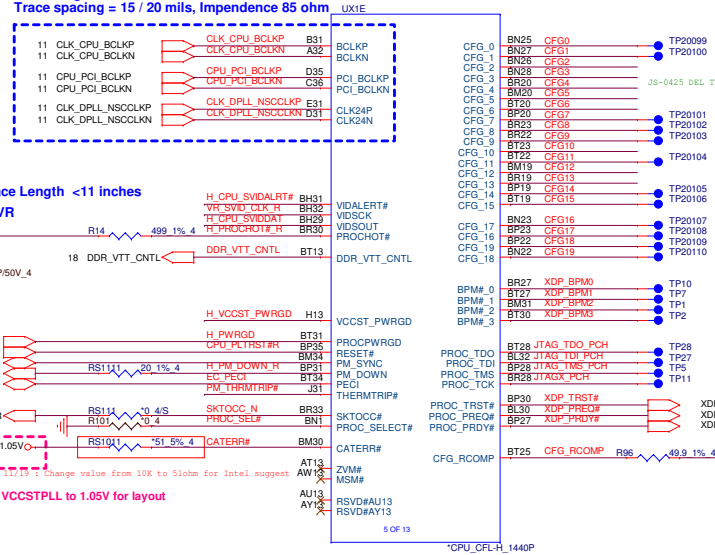


Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mil



Layout Notes:

PROCHOT# (50ohm) Trace Length <11 inches

Ca need placment near VR

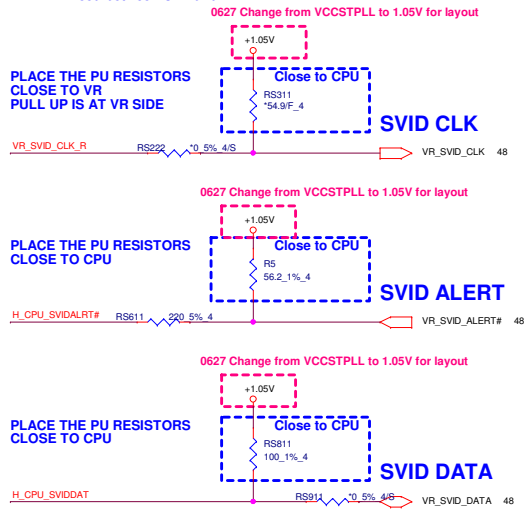
Layout Notes:

H_PWRGD (50ohm) Trace Length: 1~11 inches
CPU_PLTRST# (50ohm) Trace Length: 10~17 inches
PM_SYNC (50ohm) Trace Length: 1~11.25 inches

CPU CORE SVID

Layout Notes:

1. Need routing together
2. ALERT need between CLK and DATA.



Layout Notes:
H_VCCST_PWRGD (50ohm) Trace Length: 0.3" - 1.5"
Rc close to CPU side

Layout Notes:
THERMTRIP# (50ohm) Trace Length: 1.1~12 inches
Rb need placment near PCH

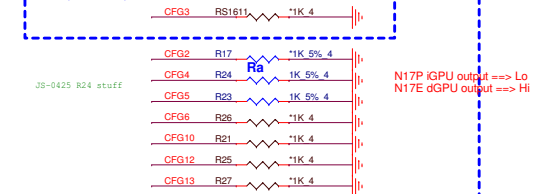
Layout Notes:
Please keep VDDQ plane is enough for 2.8A

	CFG[4]	Ra
EDP Output from DGPU	Hi	Non Stuff
EDP Output from iGPU	Low	Stuff

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a Oxm board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS for training	



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0822 follow starmade downsize

dGPU

dGPU

Layout Note: PEG_RCOMP
 Max Trace length = 600 MILS
 Min Trace width = 5 MILS
 Trace spacing to others = 15 MILS

DMI

DMI

UXIC

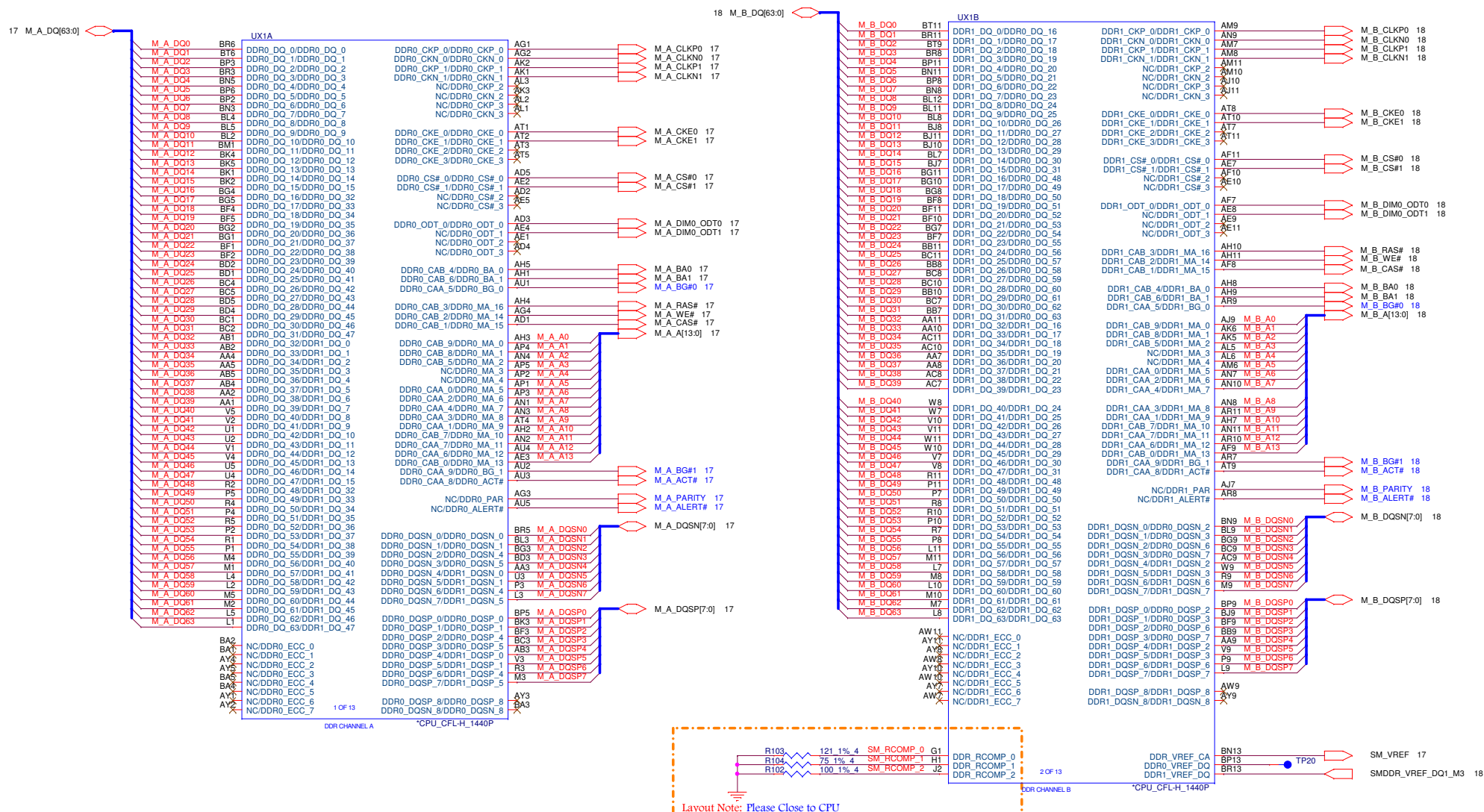
eDP

Layout Note: DISP_RCOMP
 Max Trace length = 600 MILS
 Min Trace width = 5 MILS
 Isolation Spacing = 20 MILS

dGPU only Disable intel audio

0107 unstuff

CFL-H Processor (DDR4)



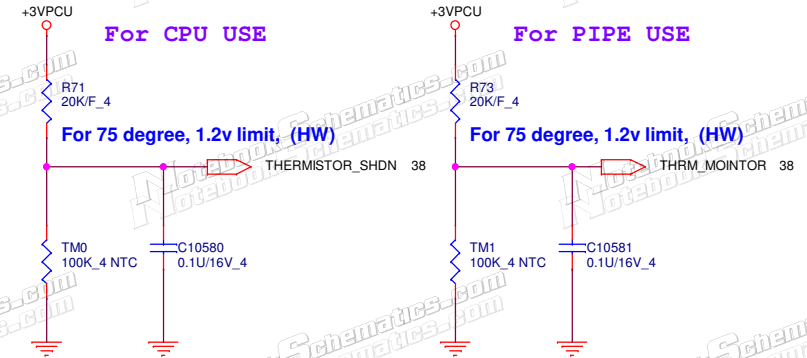
Coffee Lake Processor (POWER)

05

From CFL-H Power Map
+VCCGT lccmax = 32A
+VCCGT lccPL2 = 25A



IO Thermal Protect

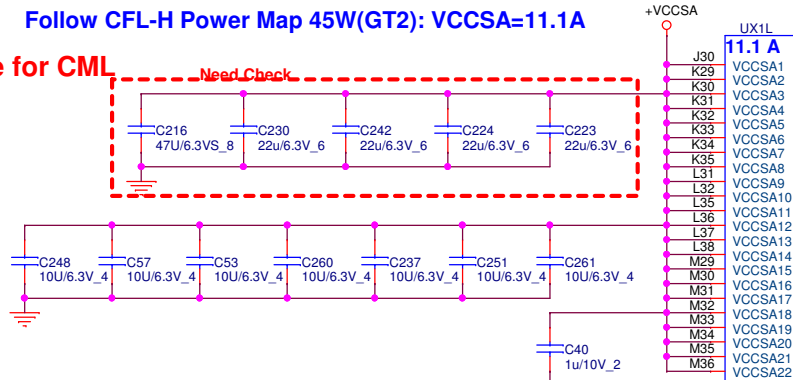


PROJECT : G3JC
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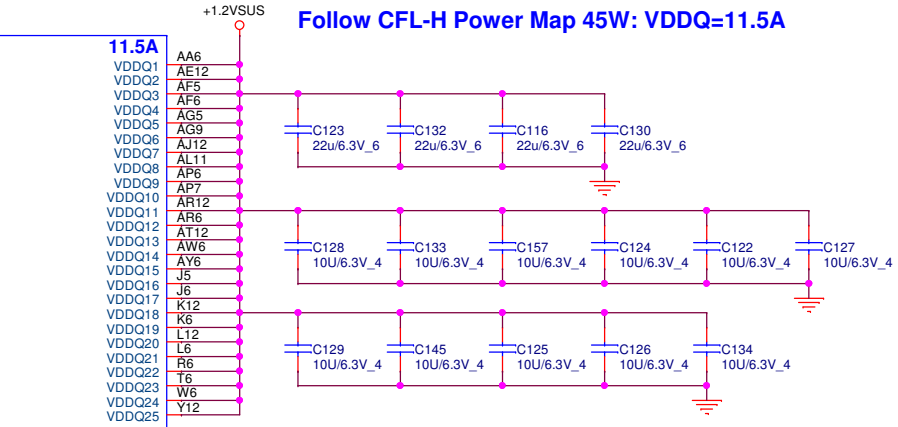
Size	Document Number	Rev
B	CFL-H 4/7 (POWER)	1A
Date: Thursday, April 23, 2020	Sheet	5 of 59

Follow CFL-H Power Map 45W(GT2): VCCSA=11.1A

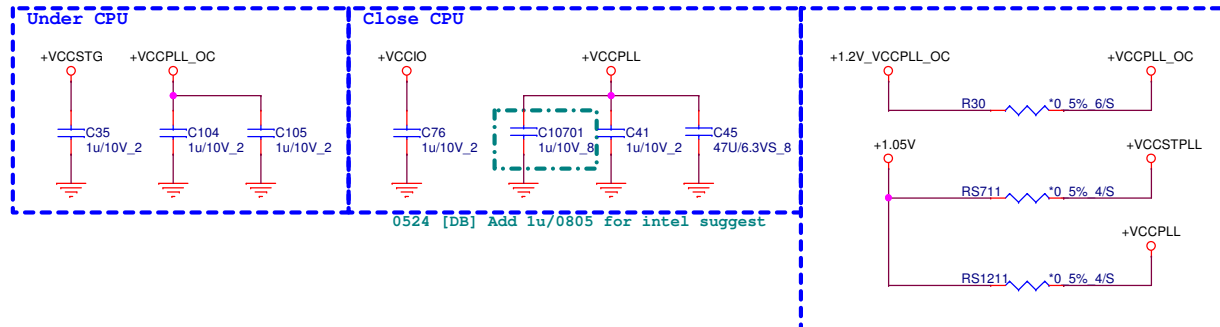
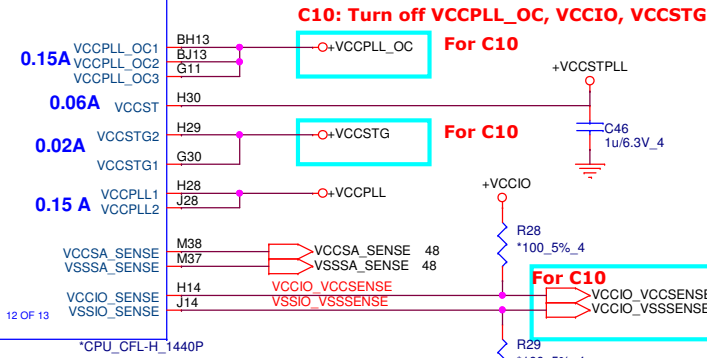
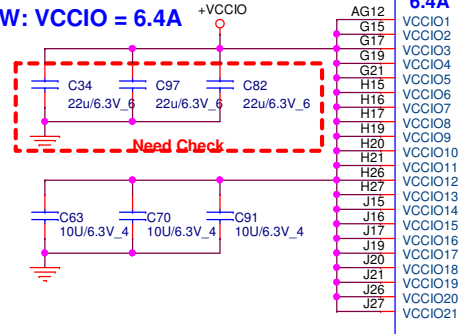
729 Change for CML



Follow CFL-H Power Map 45W: VDDQ=11.5A



Follow CFL-H Power Map 45W: VCCIO = 6.4A

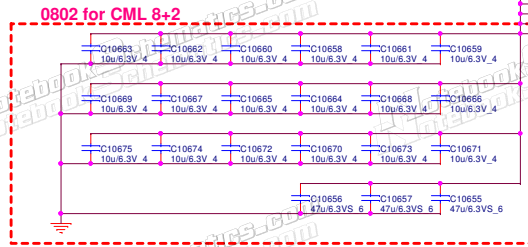
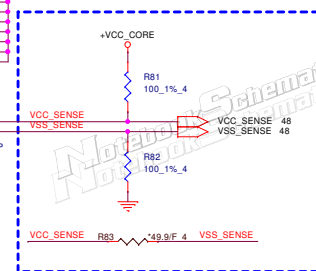
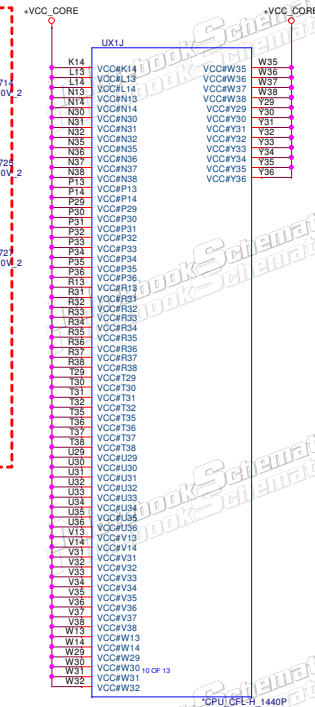


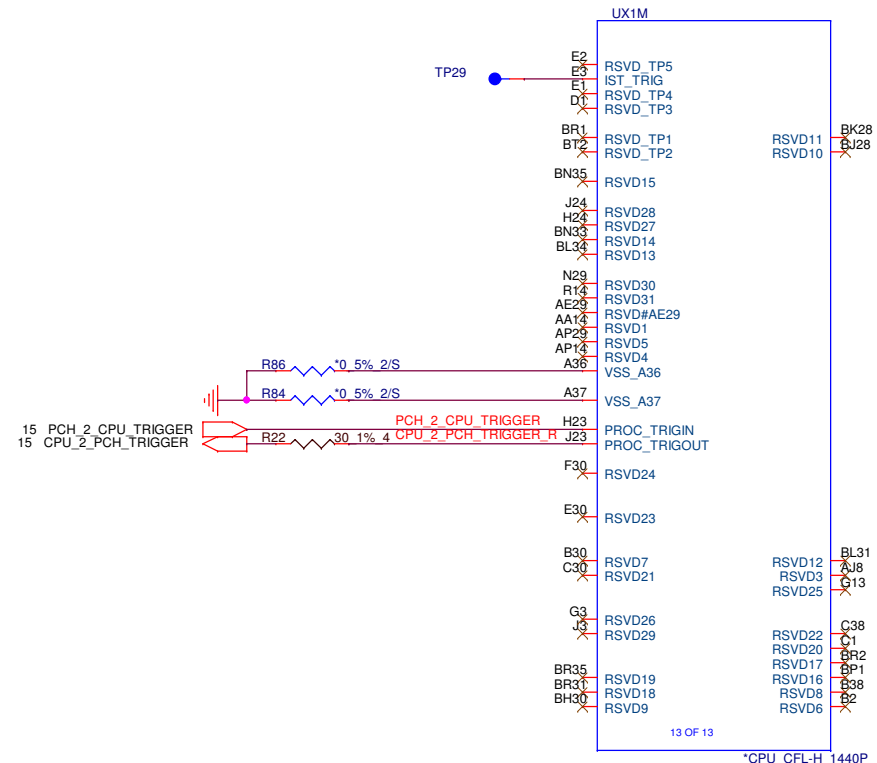
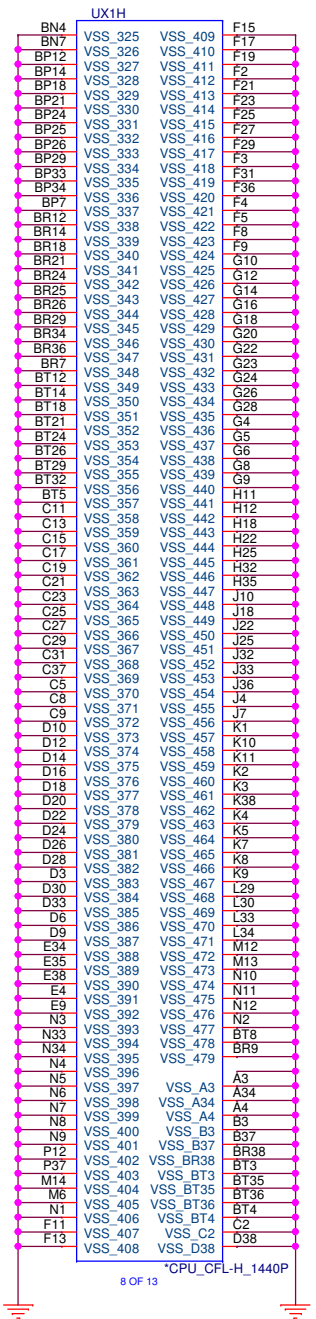
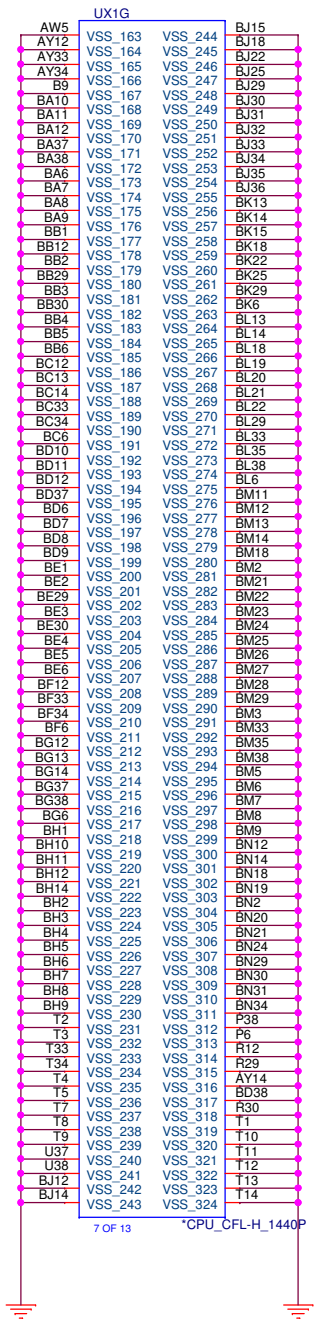
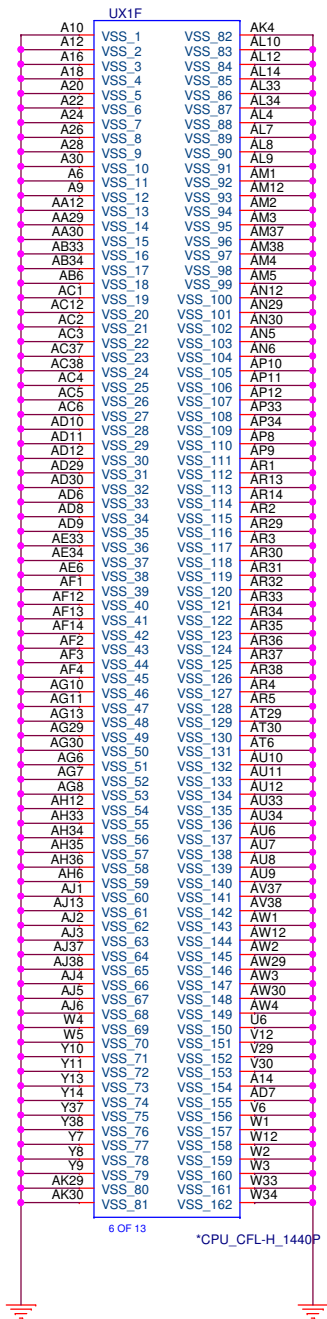
PROJECT : G3JC
Quanta Computer Inc.


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B	CFL-H 5/7 (POWER&GND)	1A
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Follow CFL-H Power Map 6 + 2 45W 80A

0729 Add & Change for CML H



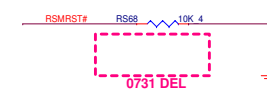
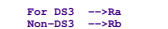




NB5

PROJECT : G3JC
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Size	Document Number	Rev
B	CFL-H 7/7 (GND)	1A
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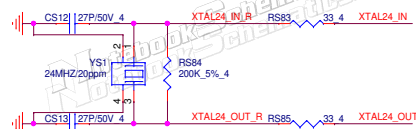
PCIe PORT	
PCIe	NC
PCIe1-8	
PCIe9	
PCIe10	SSD PCIe * 4
PCIe11	
PCIe12	SSD (SATA 1a)
PCIe13	NC
PCIe14	LAN
PCIe15	WLAN
PCIe16	CARD READER
PCIe17	1st HDD (SATA 4)
PCIe18-24	NC

SSD PCIe x4 LANE

LAN

SSD PCIe x4 (SATA1A) LANE

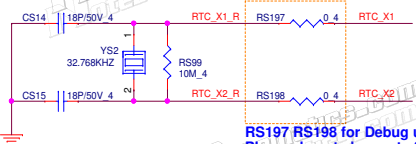
PCH Xtal 24MHz



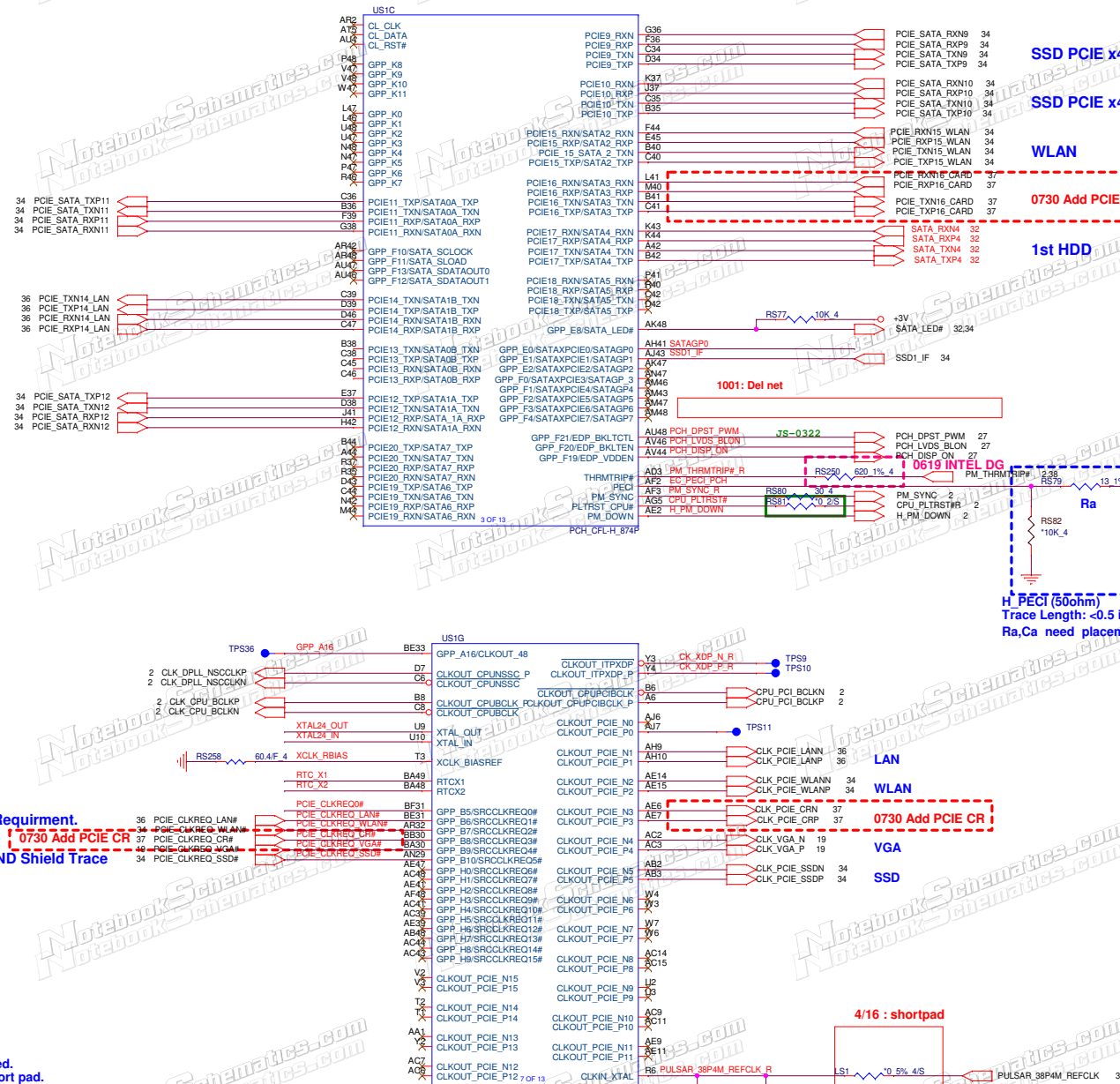
Please follow Intel CFL-H DG 571391 to meet Layout Requirement.
"12.3.2 24 MHz Input Clock Routing Guidelines"

Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out: 4-10 mil Wide GND Shield Trace

RTC Xtal 32.768KHz



RS197 RS198 for Debug used.
Please do not change to Short pad.



SSD PCIe x4 LANE

SSD PCIe x4 LANE

WLAN

0730 Add PCIe CR

1st HDD

SATAGP0
SSD1_IF
SSD1_IF: For SSD Det (SATA1A)
L: SSD PCIe IF
H: SSD SATA IF

H_PECI (50ohm)
Trace Length: <0.5 inches
Ra, Ca need placement close to PCH.

0812 downsize
0624 downsize to 0201

LAN

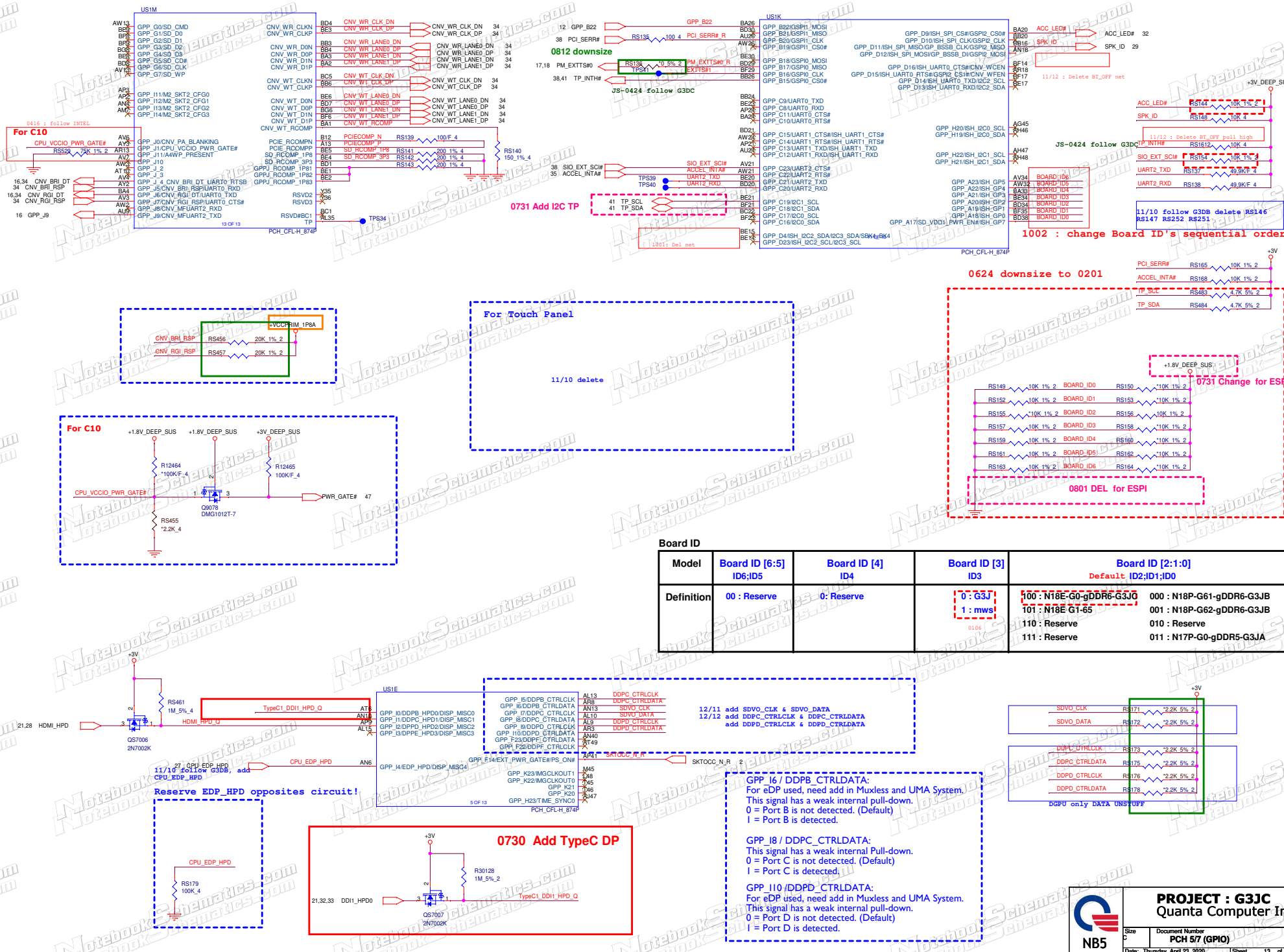
WLAN

VGA

SSD

4/16 : shortpad

Close to PCH
CS78, RS454 --> L1
L: < 8"
5" < L < 9" 2.2pF to 3.3pF
9" < L < 10" 1pF to 2.2pF



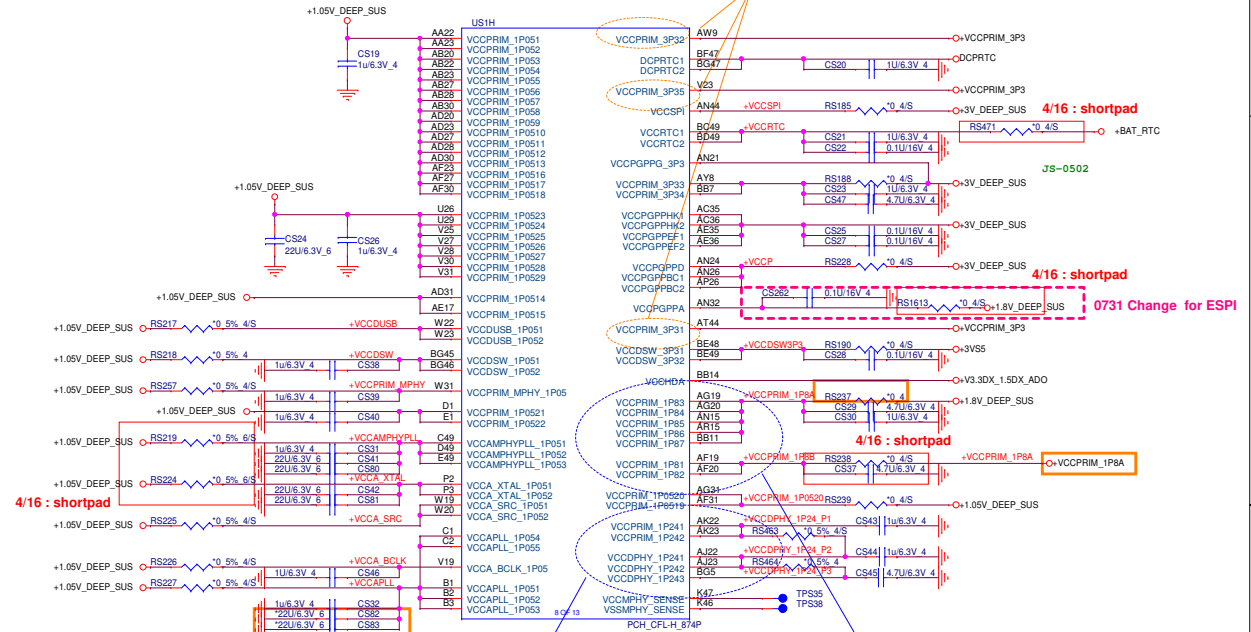
Please follow below table to check Layout

PCH-H Estimated I_{cc}^3 with Integrated 1.8V VRM Mode OFF (H Mobile SKUs)

Voltage Rail	Voltage (V)	S0 Iccmax Current ² (A)	Sx Icc Idle Current ⁴ (mA)	S0Ix Iccmax Current (mA)	Deep Sx Icc Idle Current (mA)	G3 (μA)
VCCAPLL_1P05	1.05	0.034	0.2	0.801	0	0
VCCA_BCLK_1P05	1.05	0.007	0.1	0.087	0	0
VCCA_SRC_1P05	1.05	0.141	0.3	0.838	0	0
VCCA_XTAL_1P05	1.05	0.005	0.544	0.195	0	0
VCCAMPHYPLL_1P05	1.05	0.114	0.4	1.192	0	0
VCCPRIM_1P05	1.05	4.174	40.344	0.477A	0	0
HSIO Lane Adder refer to Table 10-7 column HALO						
VCCPRIM_MPHY_1P05	1.05	0.088	0.2	1.22	0	0
VCCDSW_1P05	1.05	0.01	0.2	0.001	0.2	0
VCCDUSB_1P05	1.05	0.33	1.288	16.373	0	0
VCCHDA	3.3	0.007	0.1	4.908	0	0
VCCDSW_3P3	3.3	0.094	0.2	0.705	1.05	0
VCCPRIM_3P3	3.3	0.318	0.3	0.916	0	0
VCCPGPPA	3.3	0.085	0.1	0.103	0	0
VCCPGPPBC	3.3	0.286	0.2	0.232	0	0
VCCPGPPD	3.3	0.117	0.1	0.109	0	0
VCCPGPPEF	3.3	0.145	0.2	0.094	0	0
VCCPGPPG_3P3	3.3	0.121	0.1	0.072	0	0
VCCPGPPHK	3.3	0.219	0.2	0.138	0	0
VCCPRIM_1P8	1.8	0.152	6.607	9.411	0	0
CNVi Adder refer to Table 10-8, column HALO						
VCCRTC ¹	3.0	0.31mA	0.299	0.075	0.316	6
VCCSPI	3.3	0.042	0.1	0.153	0	0

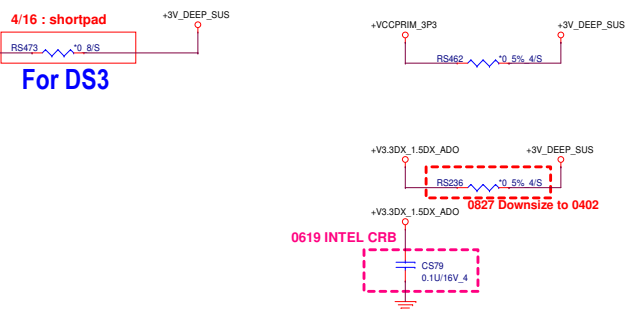
Notes:

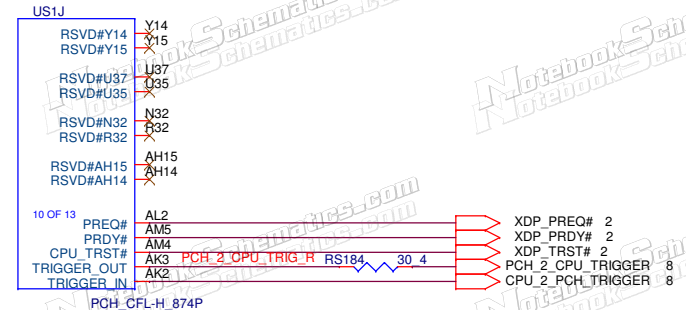
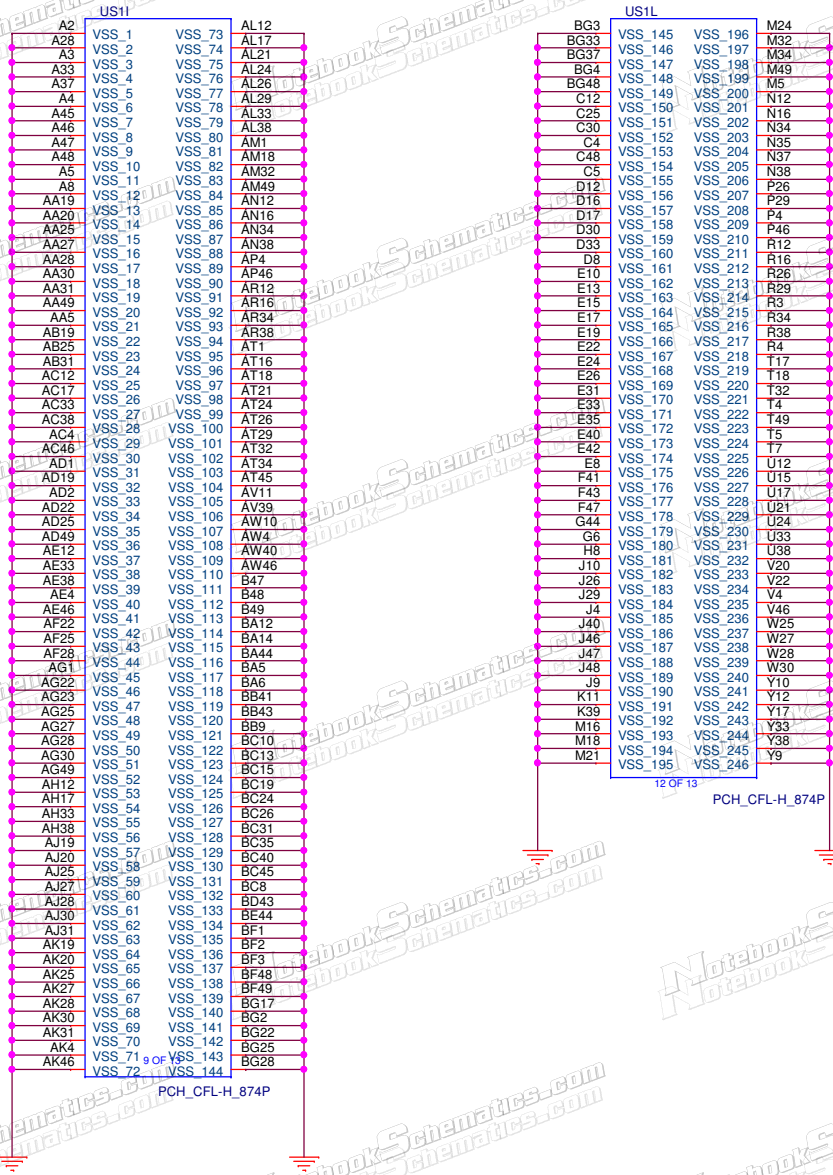
- The VCC rail ICC data is taken at 3.0V while the system is in a mechanical off (G3) state at room temperature.
- Iccmax estimates assumes 110 °C.
- The Iccmax value is a steady state current that can happen after respective power ok has asserted (or reset signal has de-asserted).
- Sx Icc Idle assumes PCH is idle and ME is power gated.
- Sx Icc at 3.3V level is assumed. Sx Icc data at the 1.8 V and/or 1.5V level not measured.



When you use external Power to provide 1.24V to CNVi, Please connect here

VCCPRIM_1P8
Without CNVi = Icc = 0mA
With CNVi = 582mA
Chipset will use this power rail to internal LDO and output 1.24V for CNVi used.





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Quanta Computer Inc.

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B	PCH 7/7 (GND)	1A
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Pin Straps (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWR0K	The signal has a weak internal pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap. Notes: 1. The internal pull-down is disabled after PCH_PWR0K is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCH, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPIO_MOSI	No Reboot	Rising edge of PCH_PWR0K	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. Notes: 1. The internal pull-down is disabled after PCH_PWR0K is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Pin Straps (Sheet 3 of 4)

Signal	Usage	When Sampled	Comment
SPIO_I03 Page12	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWR0K	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. Notes: 1. The internal pull-down is disabled after PCH_PWR0K is high. 2. This signal is in the primary well.
GPP_H12 / SMLALERT# Page12	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled).
GPP_I6 / DDPB_C-TRLDATA Page13	Display Port B Detected	Rising edge of PCH_PWR0K	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. Notes: 1. The internal pull-down is disabled after PCH_PWR0K de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_C-TRLDATA Page13	Display Port C Detected	Rising edge of PCH_PWR0K	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. Notes: 1. The internal pull-down is disabled after PCH_PWR0K de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA Page13	Display Port D Detected	Rising edge of PCH_PWR0K	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. Notes: 1. The internal pull-down is disabled after PCH_PWR0K de-asserts. 2. This signal is in the primary well.
GPP_F23 NA	Display Port F Detected	Rising edge of PCH_PWR0K	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. Notes: 1. The internal pull-down is disabled after PCH_PWR0K de-asserts. 2. This signal is in the primary well. 3. This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

TOP SWAP OVERRIDE STRAP

The signal has a weak internal pull-down.
0 = **Disable** "Top Swap" mode. (Default)
1 = **Enable** "Top Swap" mode. This inverts an address

GPP_B14



0624 downsize to 0201

NO REBOOT IF SAMPLED HIGH

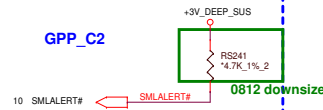
The signal has a weak internal pull-down.
0 = **Disable** "No Reboot" mode. (Default)
1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

11/10 follow G3D delete

TLS CONFIDENTIALITY ENABLED

This signal has a weak internal pull-down.
0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

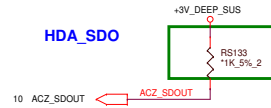
GPP_C2



0812 downsize

This signal has a weak internal pull-down.
0 = **Enable** security measures defined in the Flash Descriptor. (Default)
1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

HDA_SDO



Pin Straps (Sheet 4 of 4)

Signal	Usage	When Sampled	Comment
GPP_34 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_36 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_39	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPd7 Page9	Reserved	Rising edge of DSW_PWR0K	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

XTAL Frequency Select

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

CNV_BRI_DT

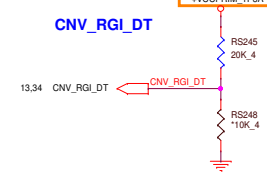


J3-0425 DEL RS249

M.2 CNVi Mode Select

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

CNV_RGI_DT

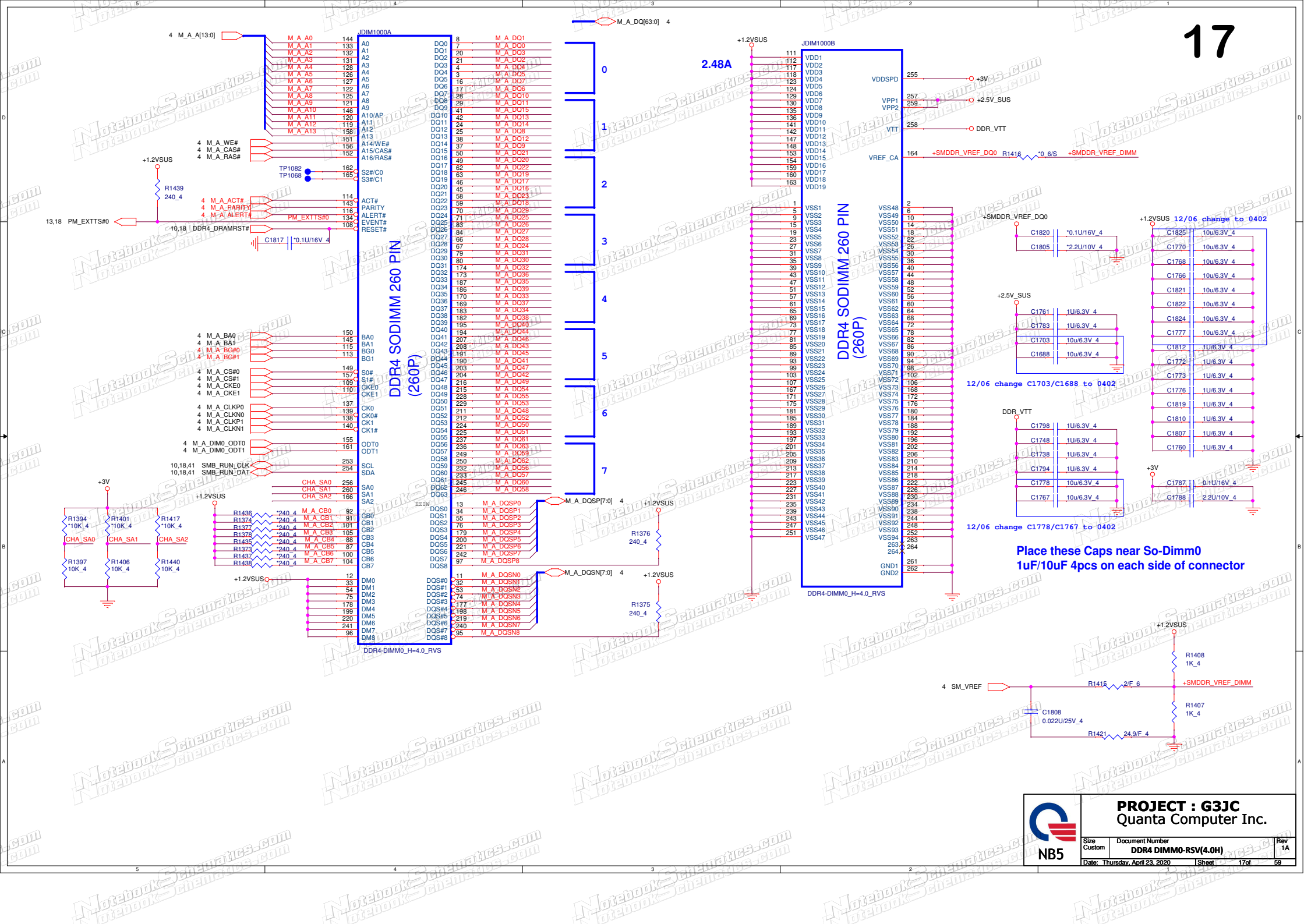


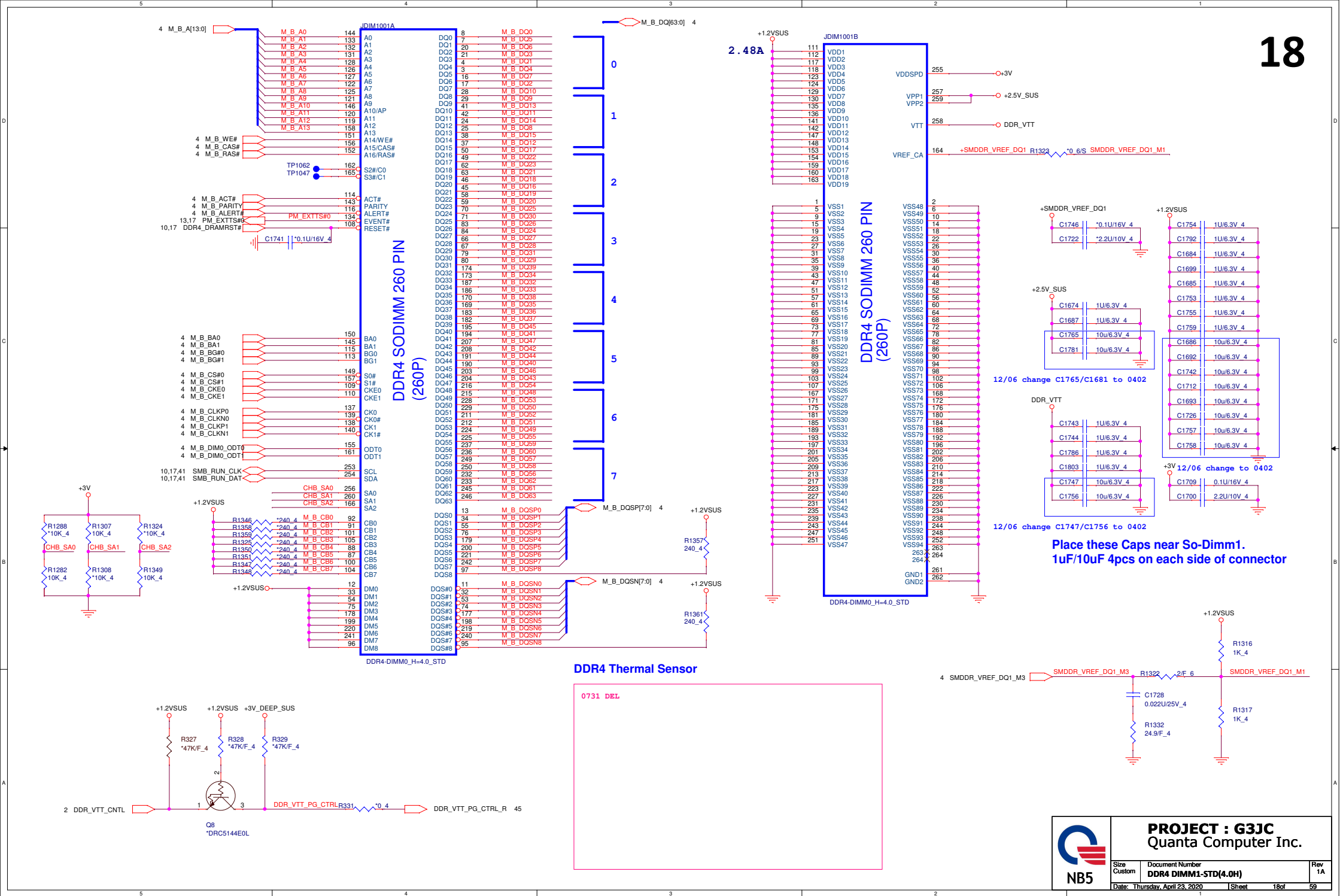
GPP_J9 1.8V VCCPSPI:

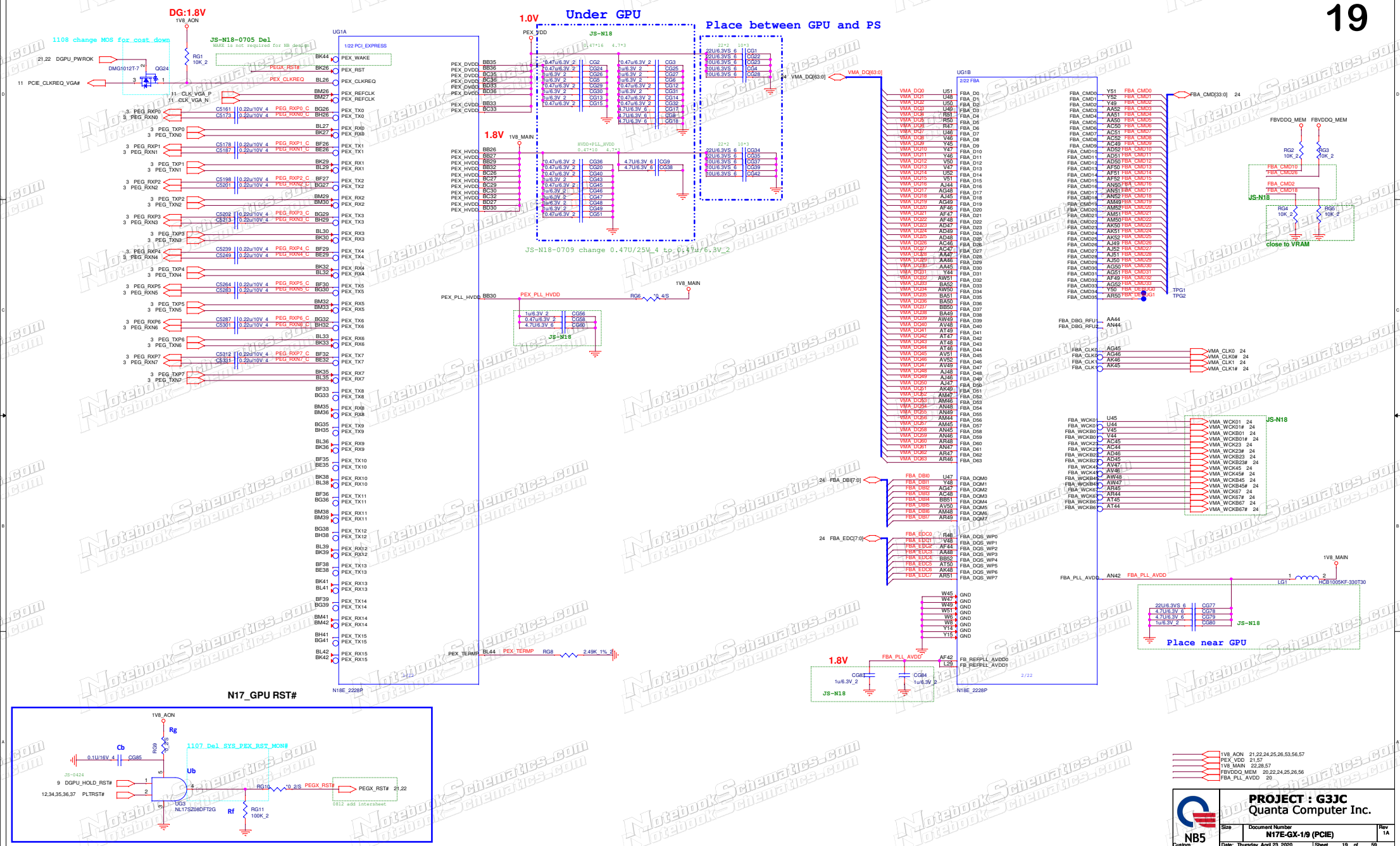
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

GPP_J9

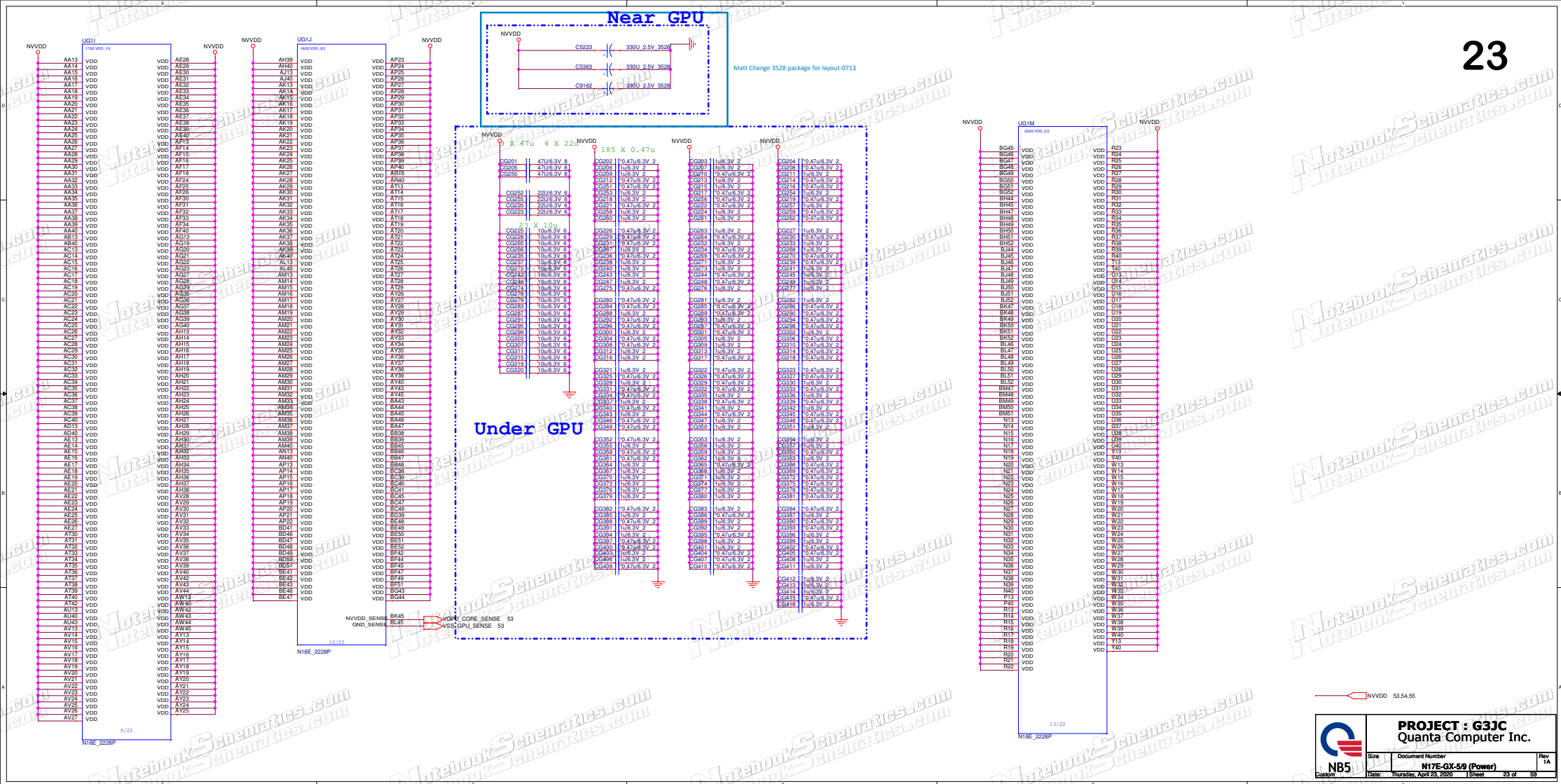




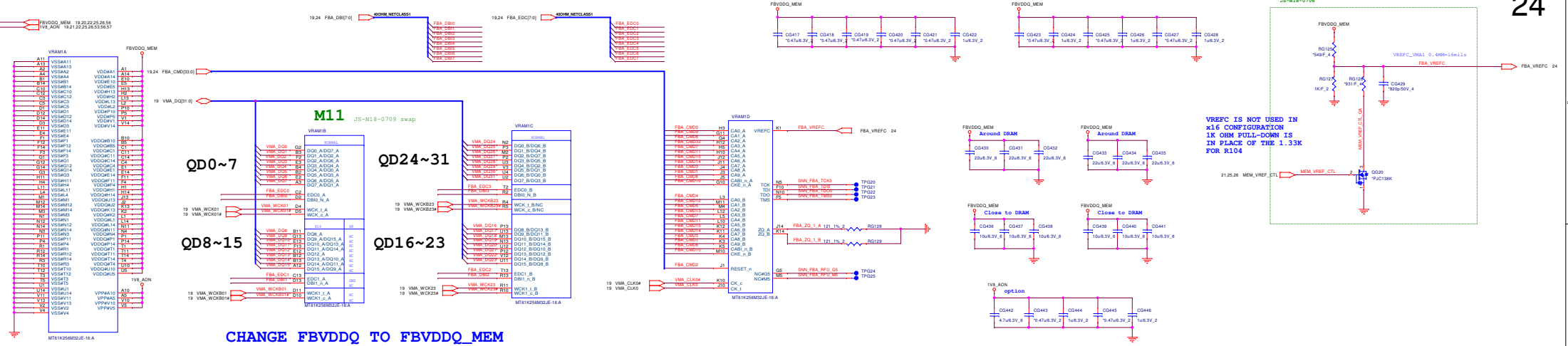




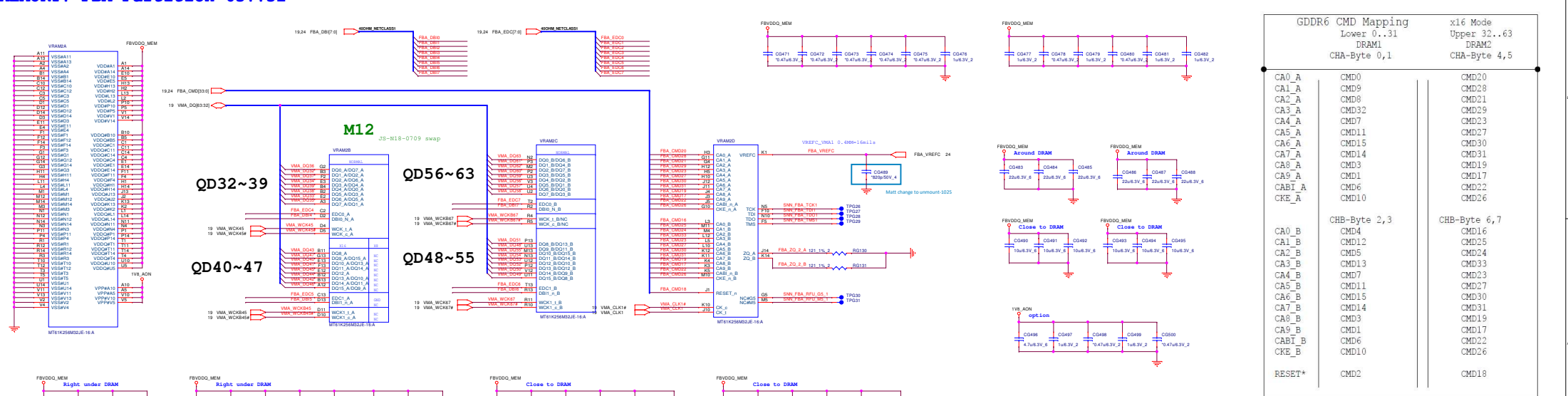




MEMORY: FBA Partition 31..00

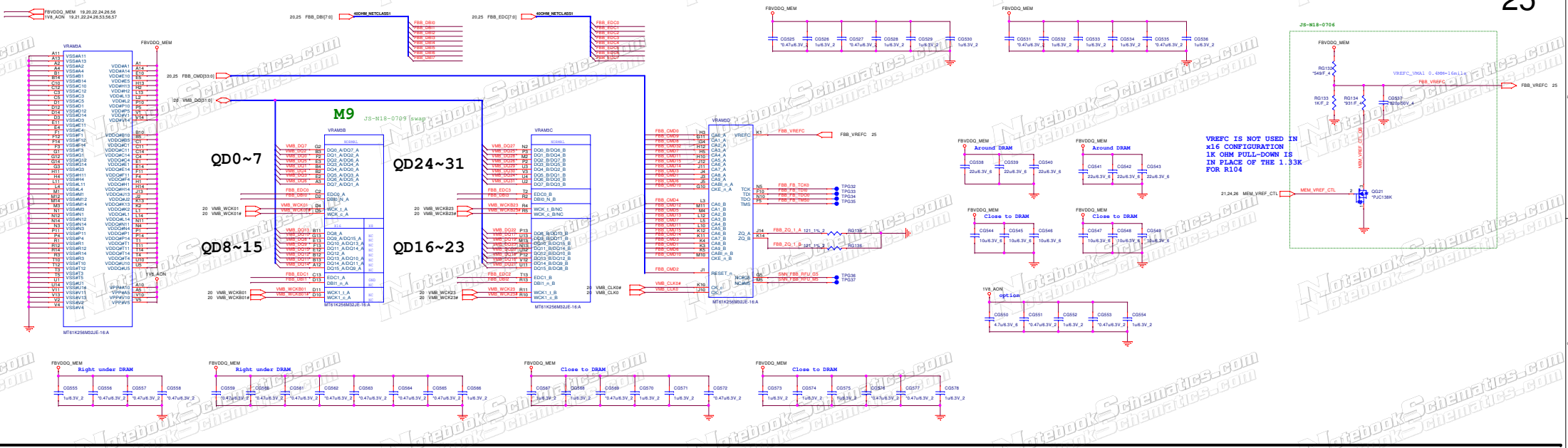


MEMORY: FBA Partition 63..32

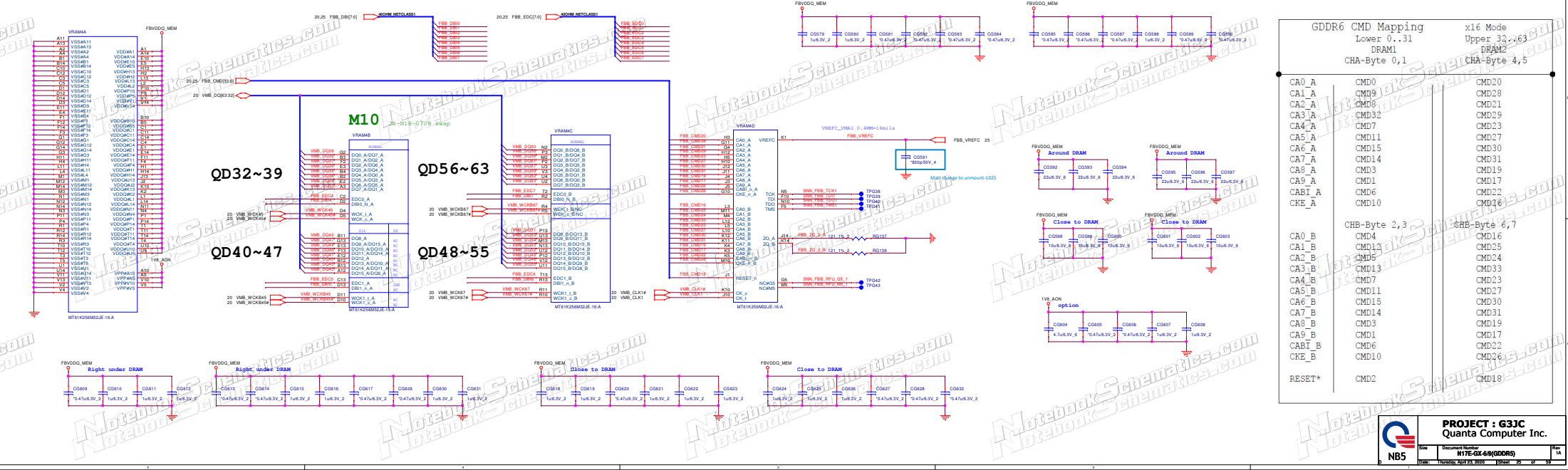


GDDR6 CMD Mapping		x16 Mode	
Lower 0..31		Upper 32..63	
CHB-Byte 0,1		CHB-Byte 4,5	
CA0_A	CMD0	CA0_A	CMD20
CA1_A	CMD9	CA1_A	CMD28
CA2_A	CMD8	CA2_A	CMD21
CA3_A	CMD32	CA3_A	CMD29
CA4_A	CMD7	CA4_A	CMD23
CA5_A	CMD11	CA5_A	CMD27
CA6_A	CMD4	CA6_A	CMD30
CA7_A	CMD14	CA7_A	CMD31
CA8_A	CMD3	CA8_A	CMD19
CA9_A	CMD1	CA9_A	CMD17
CAB1_A	CMD6	CAB1_A	CMD22
CKE_A	CMD10	CAB2_A	CMD26
CHB-Byte 2,3		CHB-Byte 6,7	
CA0_B	CMD4	CA0_B	CMD16
CA1_B	CMD12	CA1_B	CMD25
CA2_B	CMD5	CA2_B	CMD3
CA3_B	CMD13	CA3_B	CMD24
CA4_B	CMD7	CA4_B	CMD23
CA5_B	CMD11	CA5_B	CMD27
CA6_B	CMD15	CA6_B	CMD30
CA7_B	CMD14	CA7_B	CMD31
CA8_B	CMD3	CA8_B	CMD19
CA9_B	CMD1	CA9_B	CMD17
CAB1_B	CMD6	CAB1_B	CMD22
CKE_B	CMD10	CAB2_B	CMD26
RESET*		CMD18	

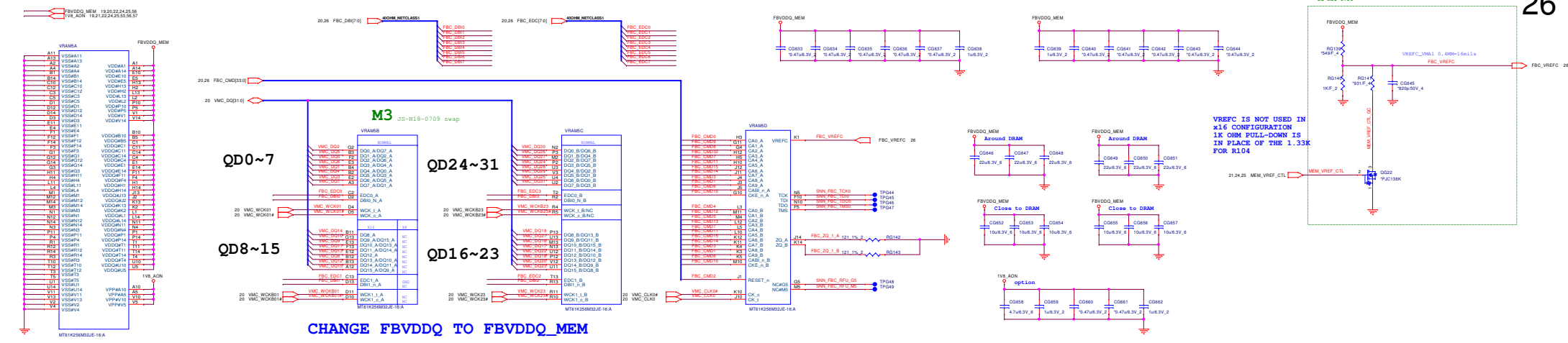
MEMORY: FBB Partition 31..0



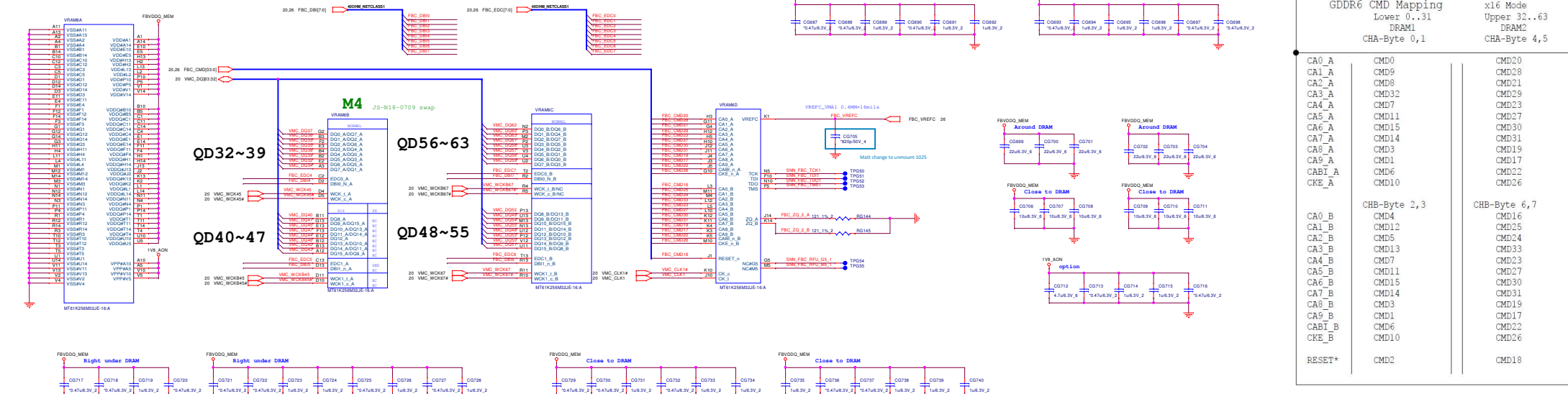
MEMORY: FBB Partition 63..32



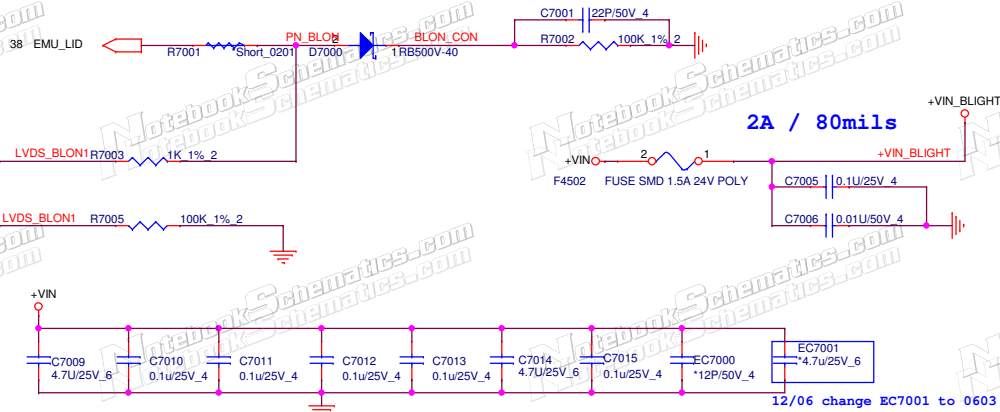
MEMORY: FBC Partition 31..0



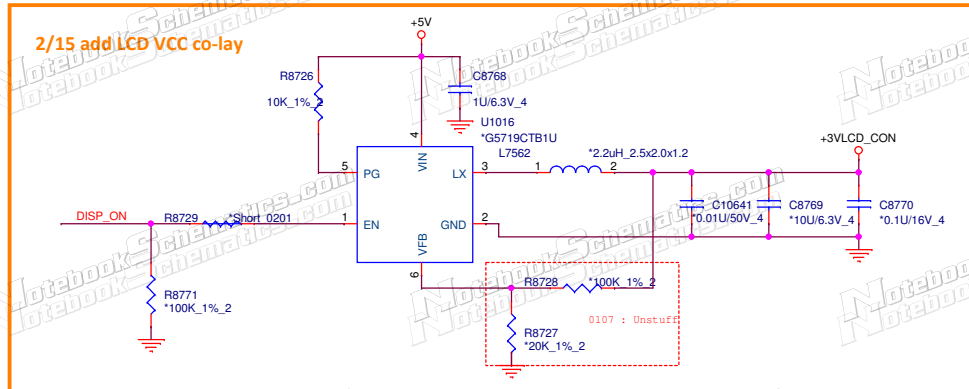
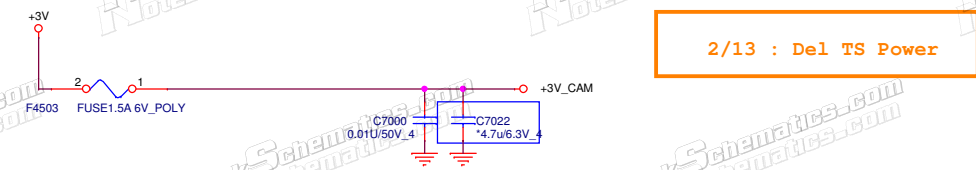
MEMORY: FBC Partition 63..32



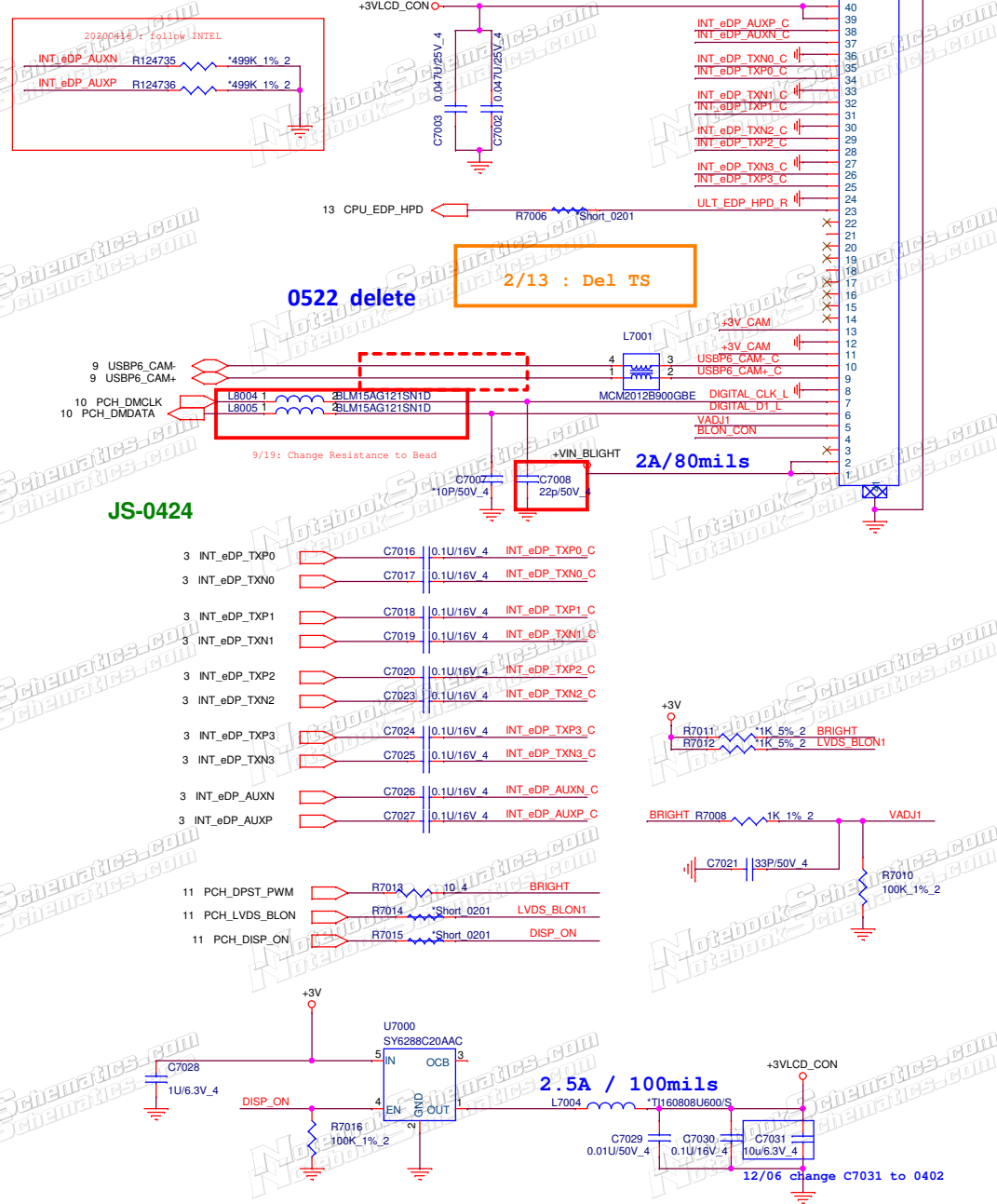
LID Switch



Touch screen



eDP Conn.



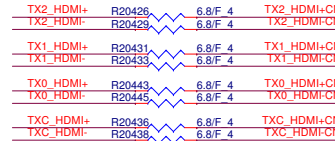
9,10,11,13,16,17,18,21,27,29,32,34,35,36,37,38,40,41,48,52,53,54,55,56,57

+3V

27,29,32,35,40,49,50,51,52,58

+5V

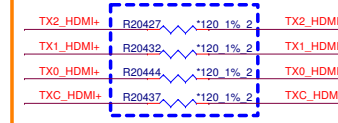
01/11 change to 0 ohm for NV suggest



1/11 modify for HDMI2.0

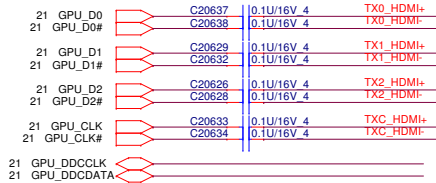
01/11 unstuff for HDMI output from GPU

EMI Solution



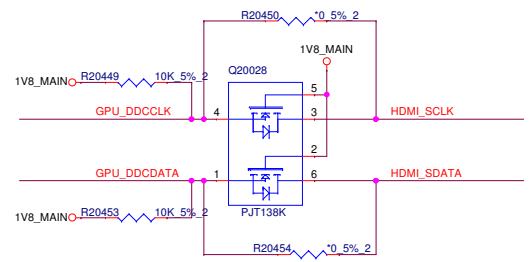
11/04 modify for HDMI2.0

11/03 modify for HDMI2.0

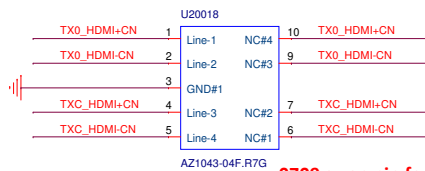


HDMI SMBus Isolation

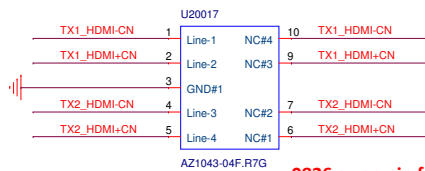
Close to HDMI connector



ESD



0709 swap pin for layout



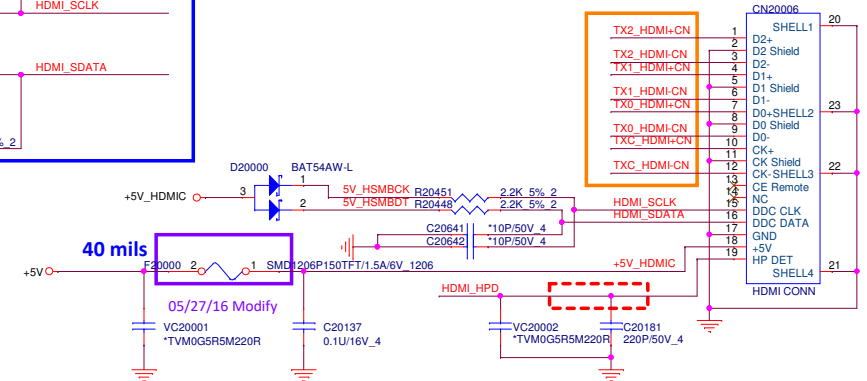
0826 swap pin for layout

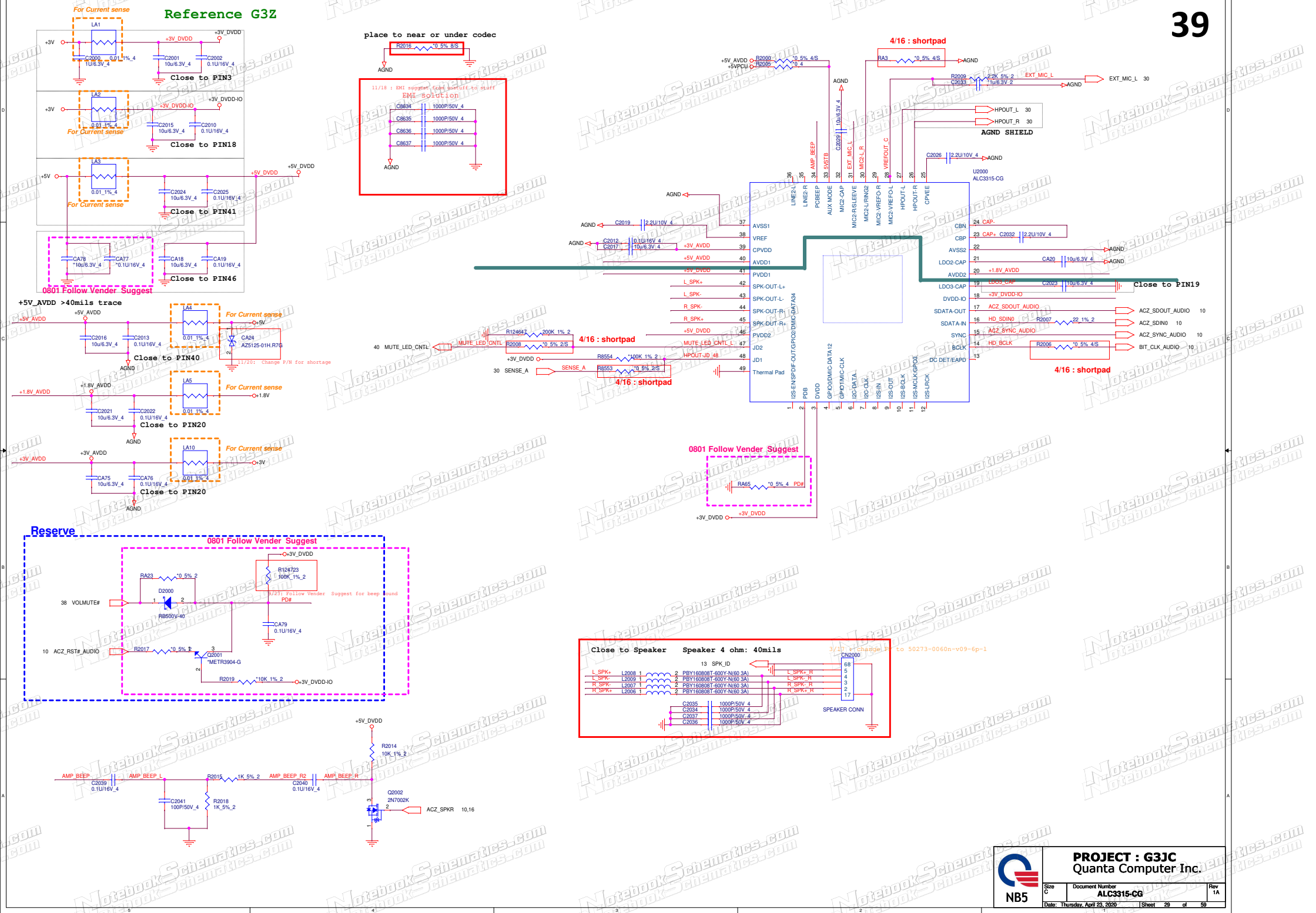
1125 Reserve ESD protection component

1125 SWAP

02/08 U20018、U20017 change to BC001043Z00 by sourcer suggest

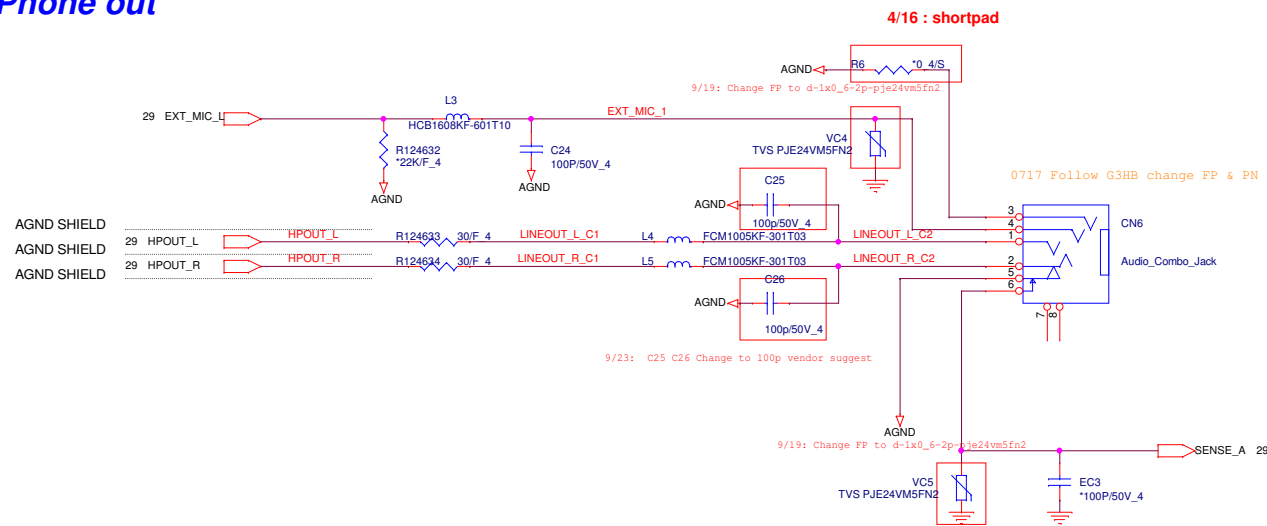
01/15 update to DFHD19MR440





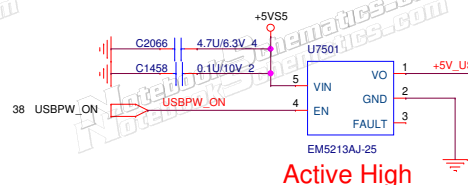
Head Phone out

30

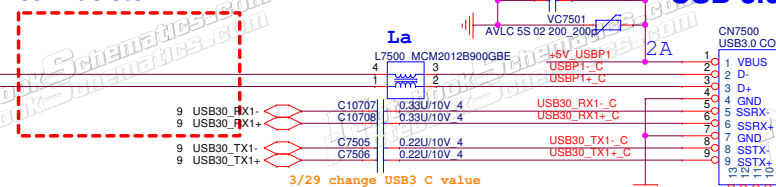


HOLE

USB BC1.2

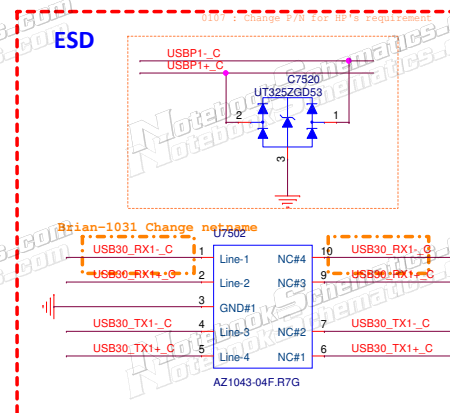


0522 delete



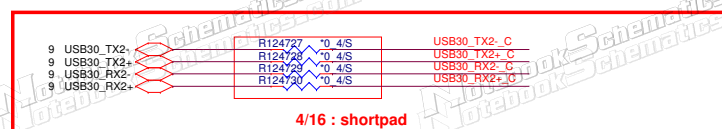
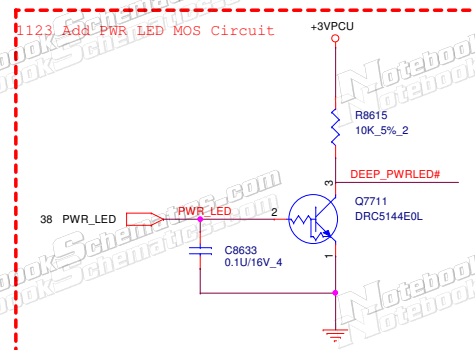
01/15 update footprint to
ub3-tcra1-9u6391-9p
02/08 change CN7500 to DFHS09FR724

ESD

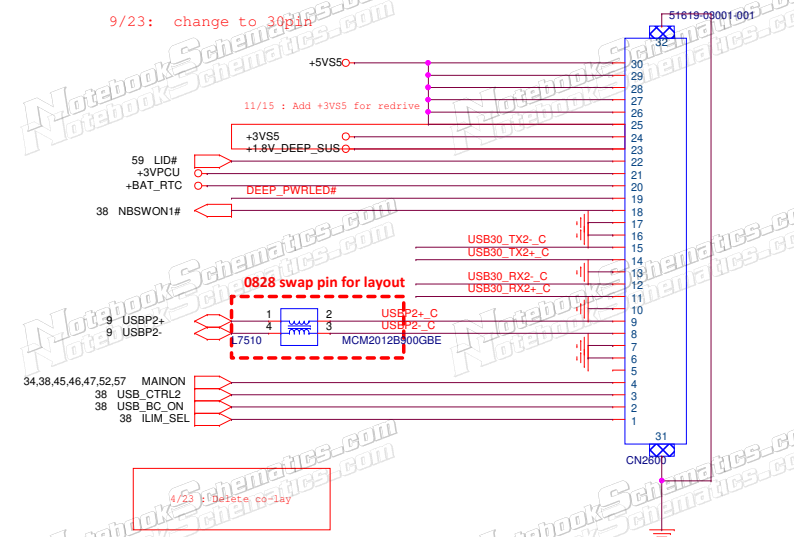


Daughter Board

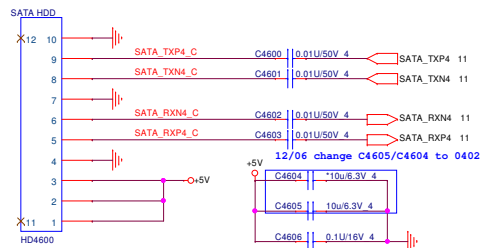
Power LED



1004 : Change Cap to resistance due to small board have been add the cap



HDD



SATA LED

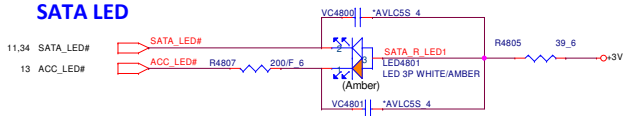


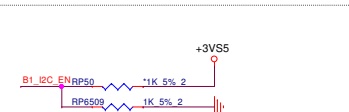
Table 7. TUSB546-DCI Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS				USB 3.1 UPSTREAM FACING PORT				ALL DISPLAYPORT LANES			
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)			
0	0	0	0.2	0	0	-1.6	0	0	1.0			
1	0	R	1.2	0	R	-0.5	0	R	3.3			
2	0	F	2.2	0	F	0.5	0	F	4.9			
3	0	1	3.3	0	1	1.6	0	1	6.5			
4	R	0	4.2	R	0	2.4	R	0	7.5			
5	R	R	5.1	R	R	3.4	R	R	8.6			
6	R	F	5.9	R	F	4.1	R	F	9.5			
7	R	1	6.7	R	1	4.9	R	1	10.4			
8	F	0	7.4	F	0	5.7	F	0	11.1			
9	F	R	8.1	F	R	6.4	F	R	11.7			
10	F	F	8.7	F	F	6.9	F	F	12.3			
11	F	1	9.3	F	1	7.5	F	1	12.8			
12	1	0	9.7	1	0	8.0	1	0	13.2			
13	1	R	10.2	1	R	8.5	1	R	13.6			
14	1	F	10.6	1	F	8.9	1	F	14.0			
15	1	1	11.1	1	1	9.4	1	1	14.4			

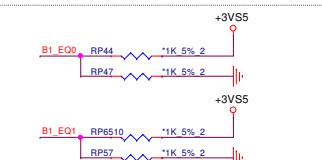
TUSB546 Pin Control Mode

CTL1	CTL0	FLIP	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

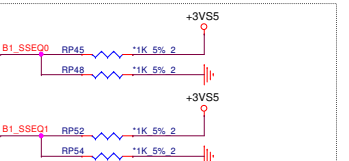
MUX TUSB546I



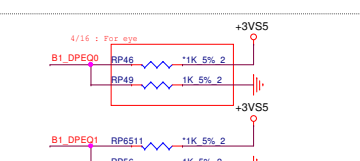
I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable) (Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V



EQ0, EQ1 : USB receiver equalizer gain
for downstream facing RX1 & RX2
F, F(Default)
F, F(Default)

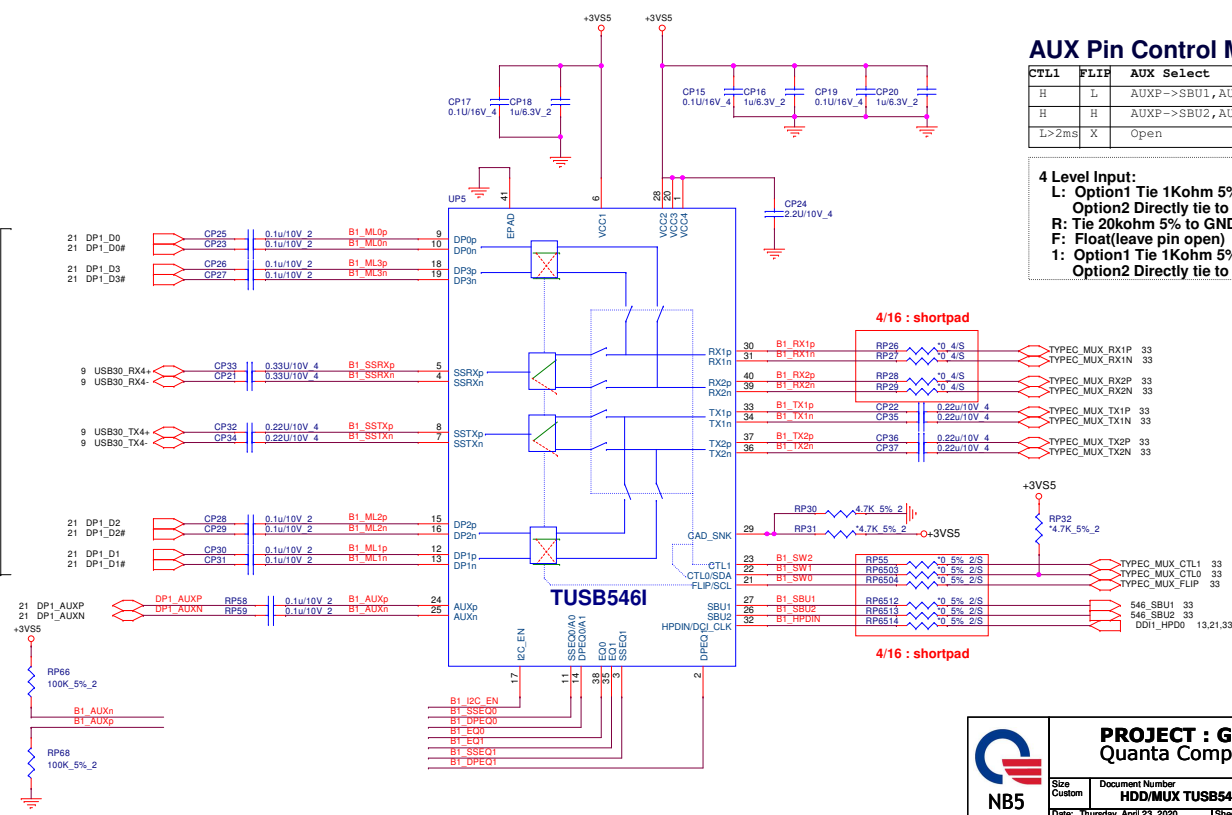


SSEQ0, SSEQ1 : USB receiver equalizer gain
for upstream facing SSTXP/N
F, F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C address



DPEQ0, DPEQ1 : DP Receiver equalization gain
F, F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C address

GPU DP1



AUX Pin Control Mode

CTL1	FLIP	AUX Select
H	L	AUXP->SBU1, AUXN->SBU2
H	H	AUXP->SBU2, AUXN->SBU1
L>2ms	X	Open

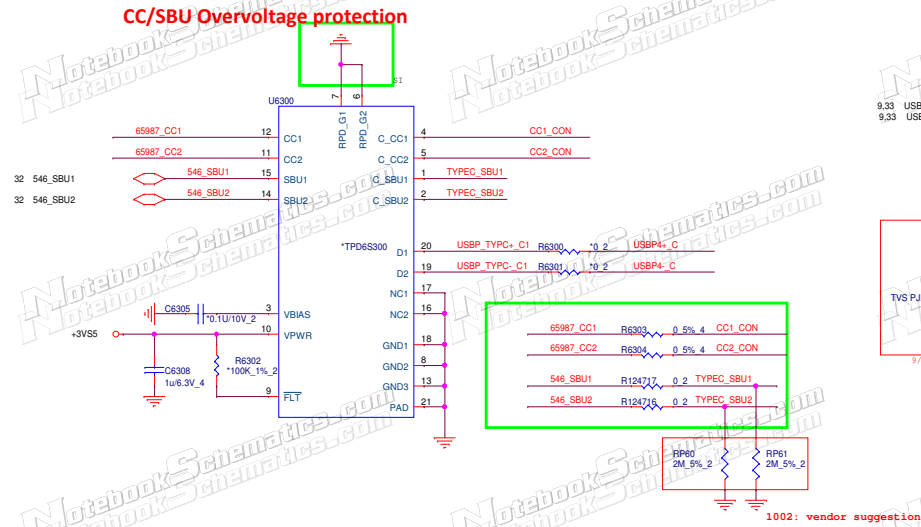
4 Level Input:
L: Option1 Tie 1Kohm 5% to GND
Option2 Directly tie to GND
R: Tie 20kohm 5% to GND
F: Float(leave pin open)
1: Option1 Tie 1Kohm 5% to Vcc
Option2 Directly tie to Vcc



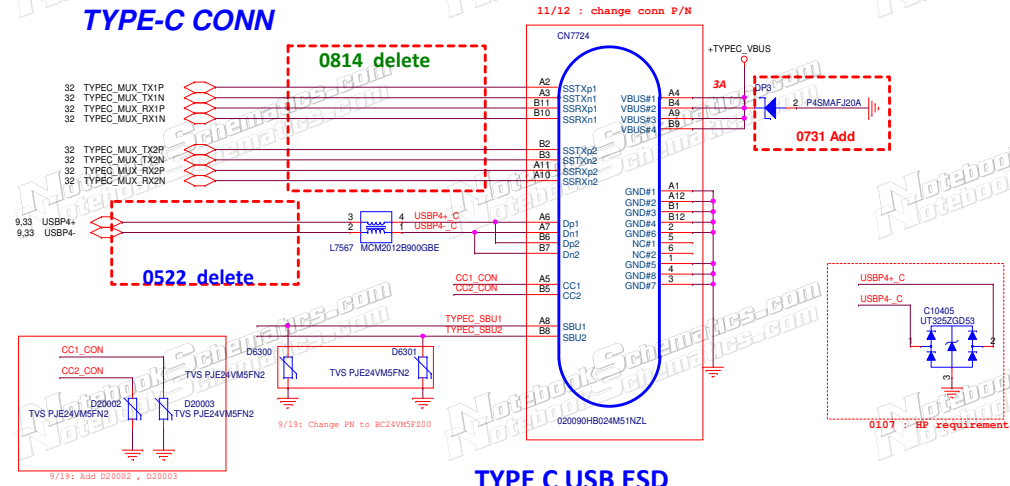
PROJECT : G3JC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/MUX TUSB546I	1A
Date: Thursday, April 23, 2020	Sheet	32of 59

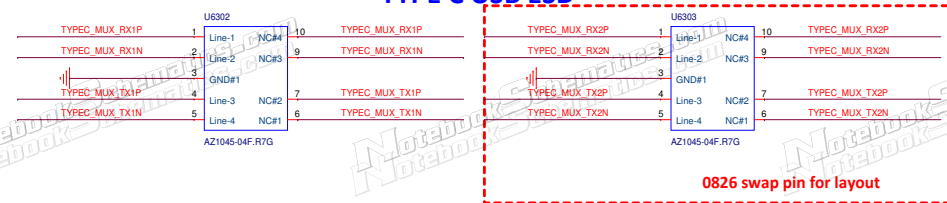
TYPE-C



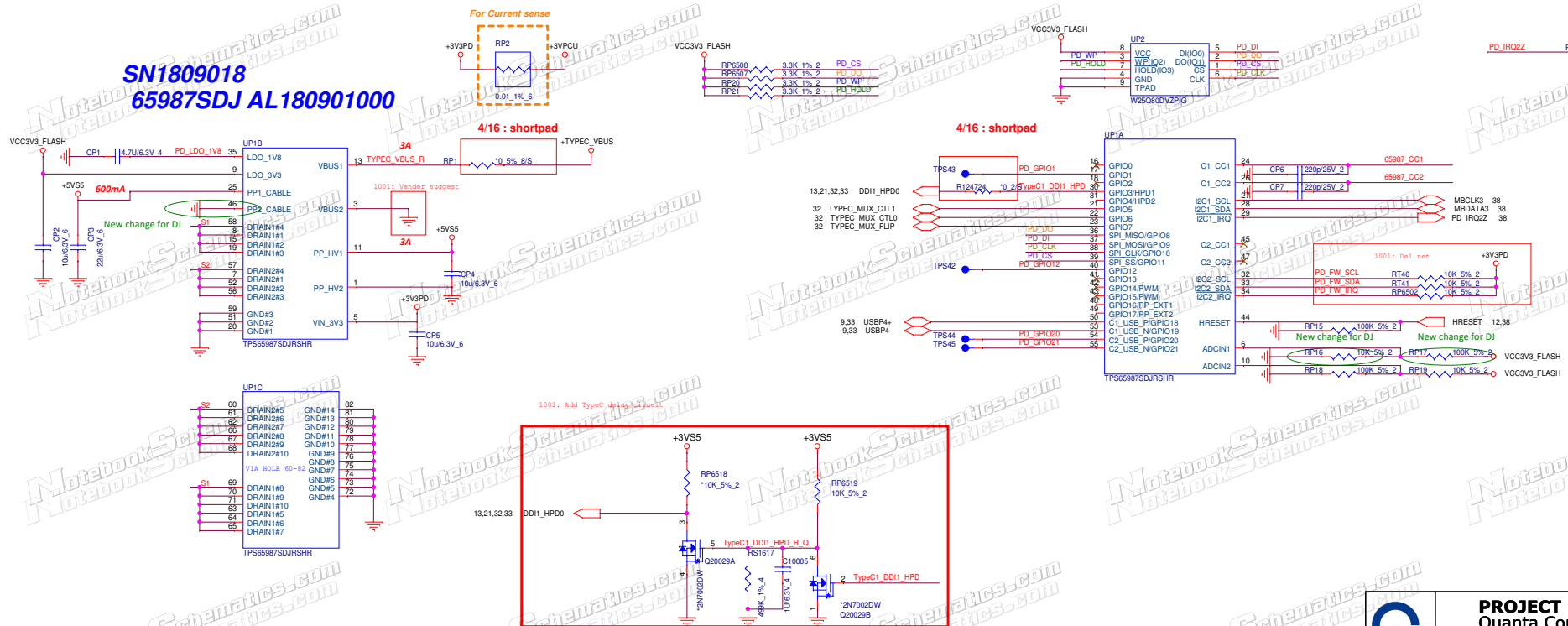
TYPE-C CONN

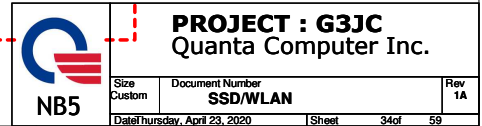


TYPE C USB ESD



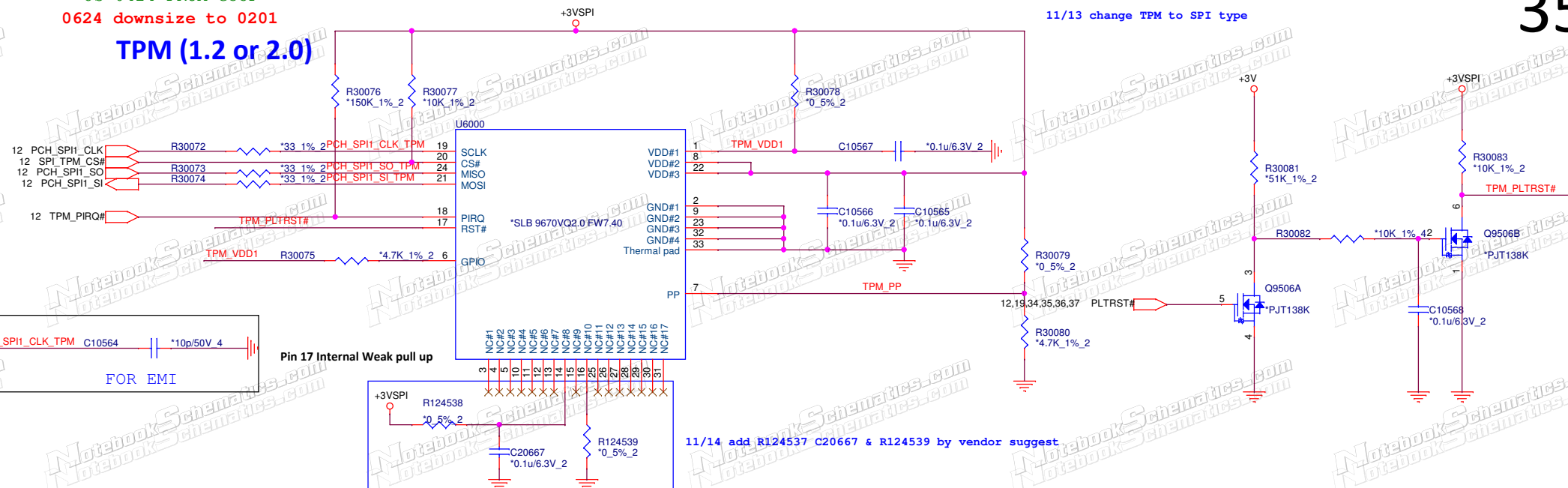
SN1809018
65987SDJ AL180901000





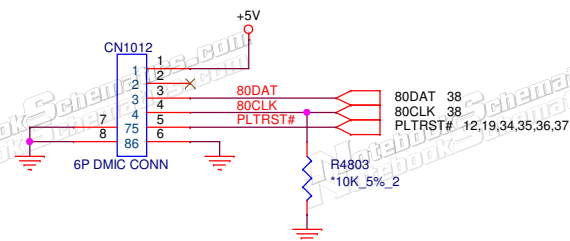
JS-0424 FROM G35P
0624 downsize to 0201

TPM (1.2 or 2.0)

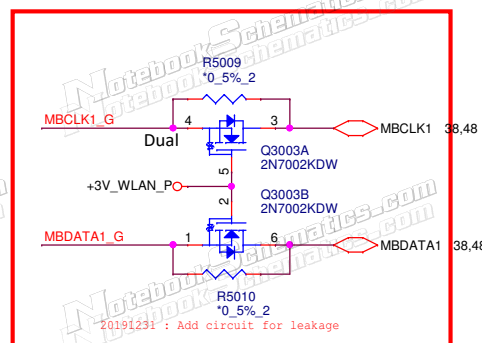
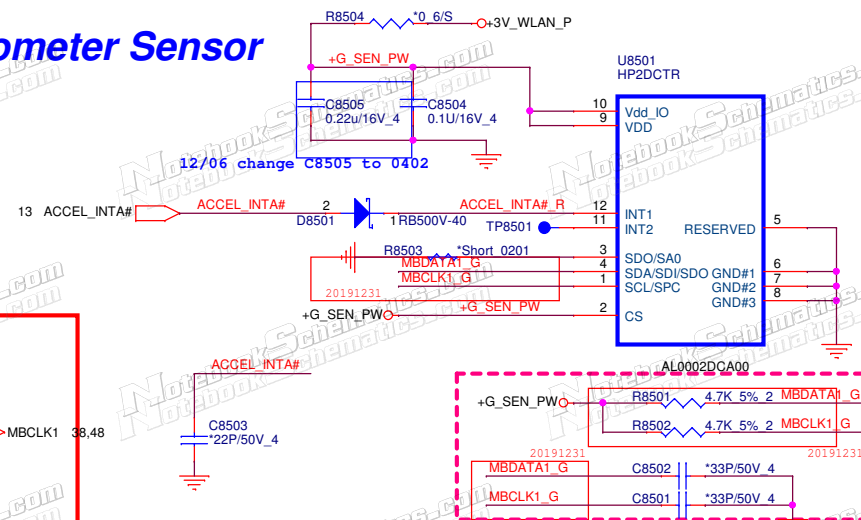


0801 Follow G3EA

For debug

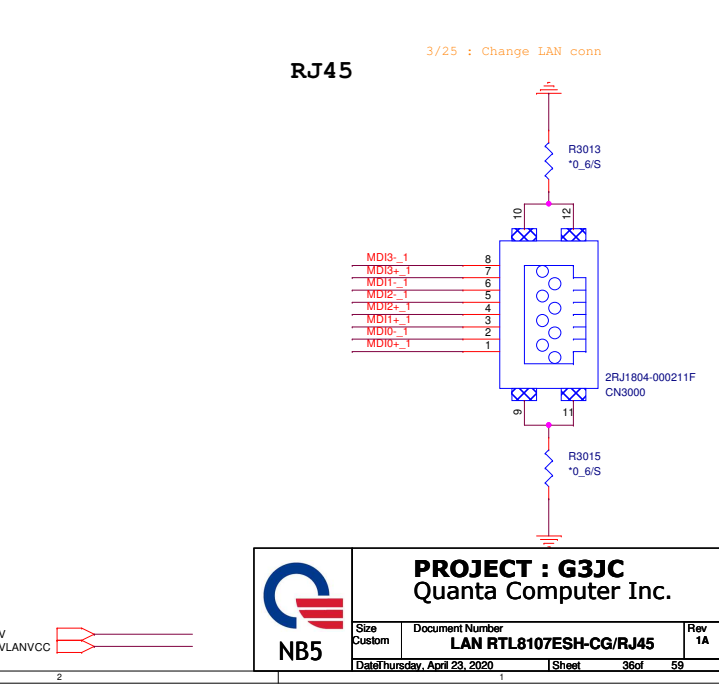
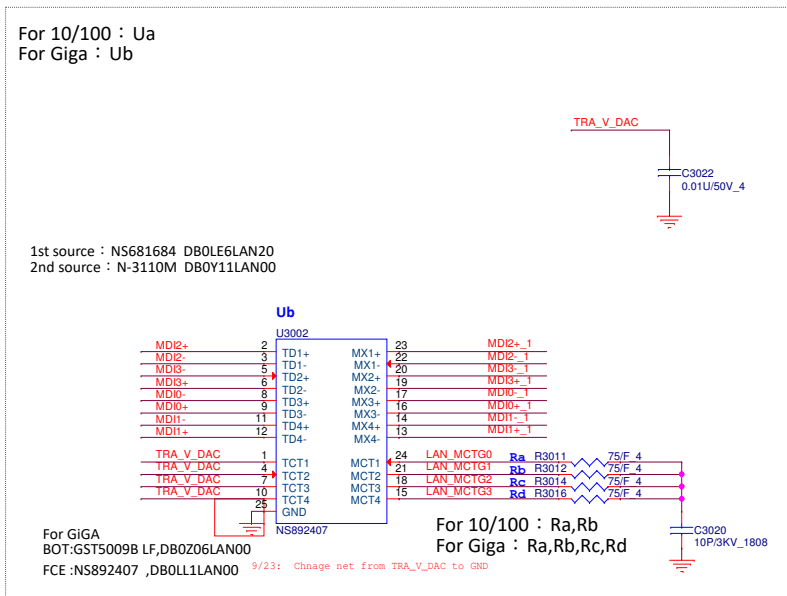
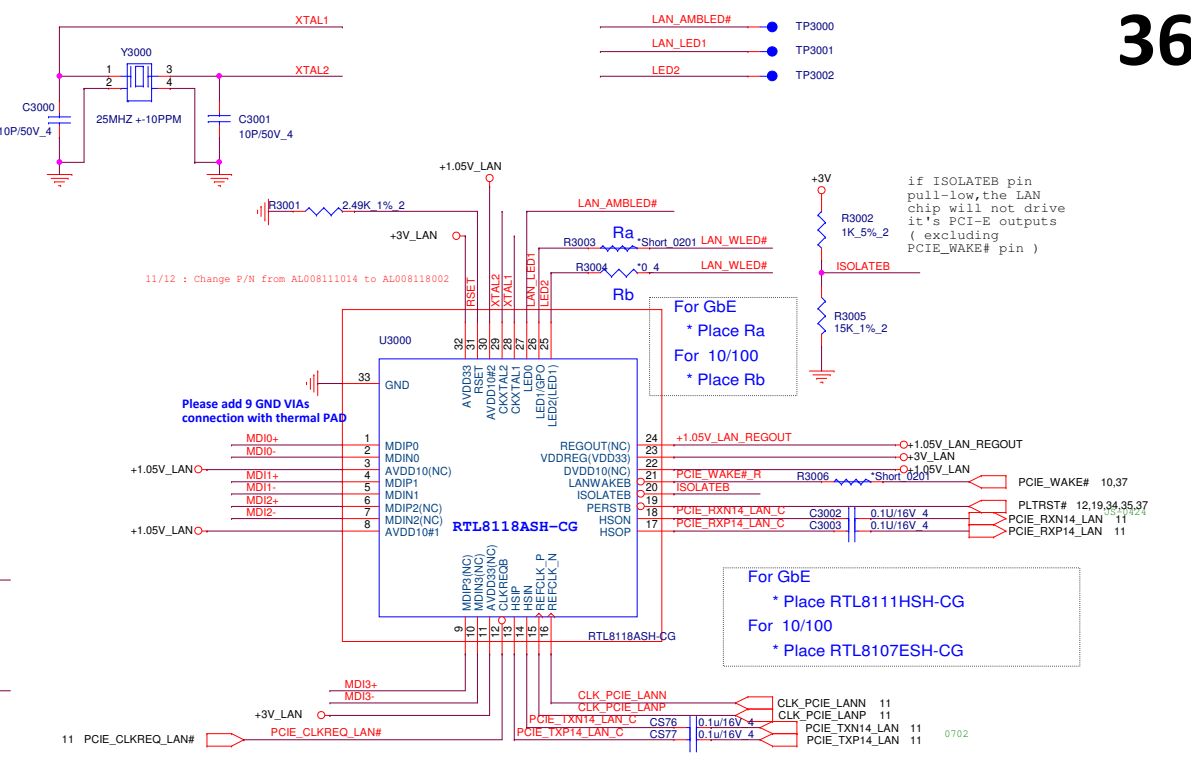


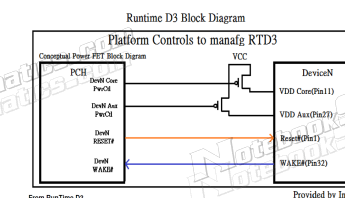
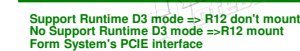
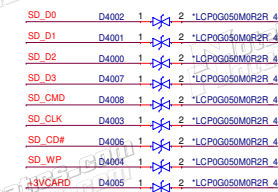
Accelerometer Sensor



PROJECT : G3JC
Quanta Computer Inc.

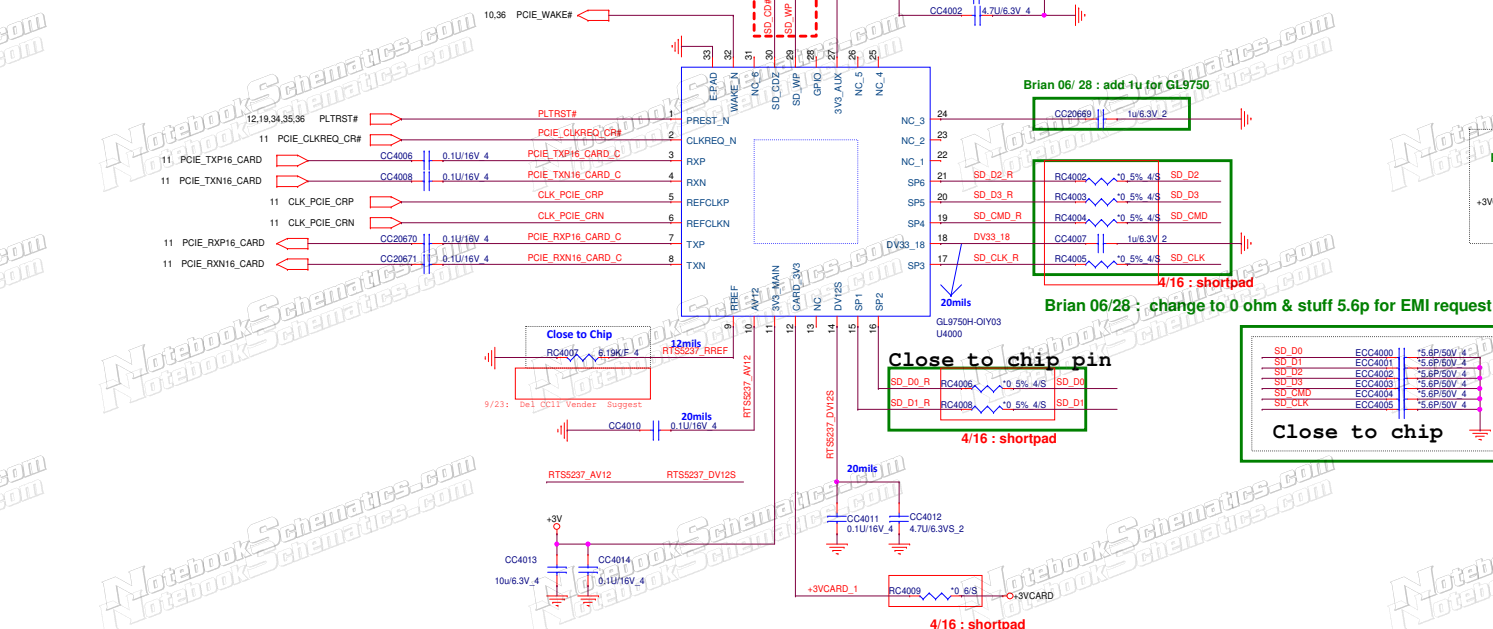
Size B	Document Number TPM/IR CAM/Sensor	Rev 1A
Date	Thursday, April 23, 2020	Sheet 35 of 59



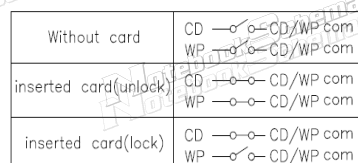


PROJECT : G3JC
Quanta Computer Inc.

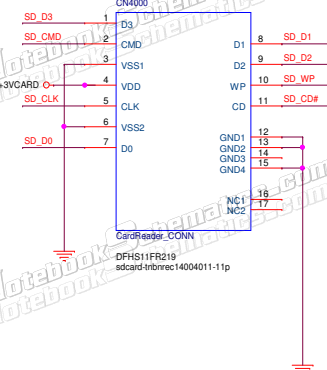
Size C	Document Number CR RTS5237S/CR SOCKET
Date Thursday, April 23, 2020	Sheet 37 of

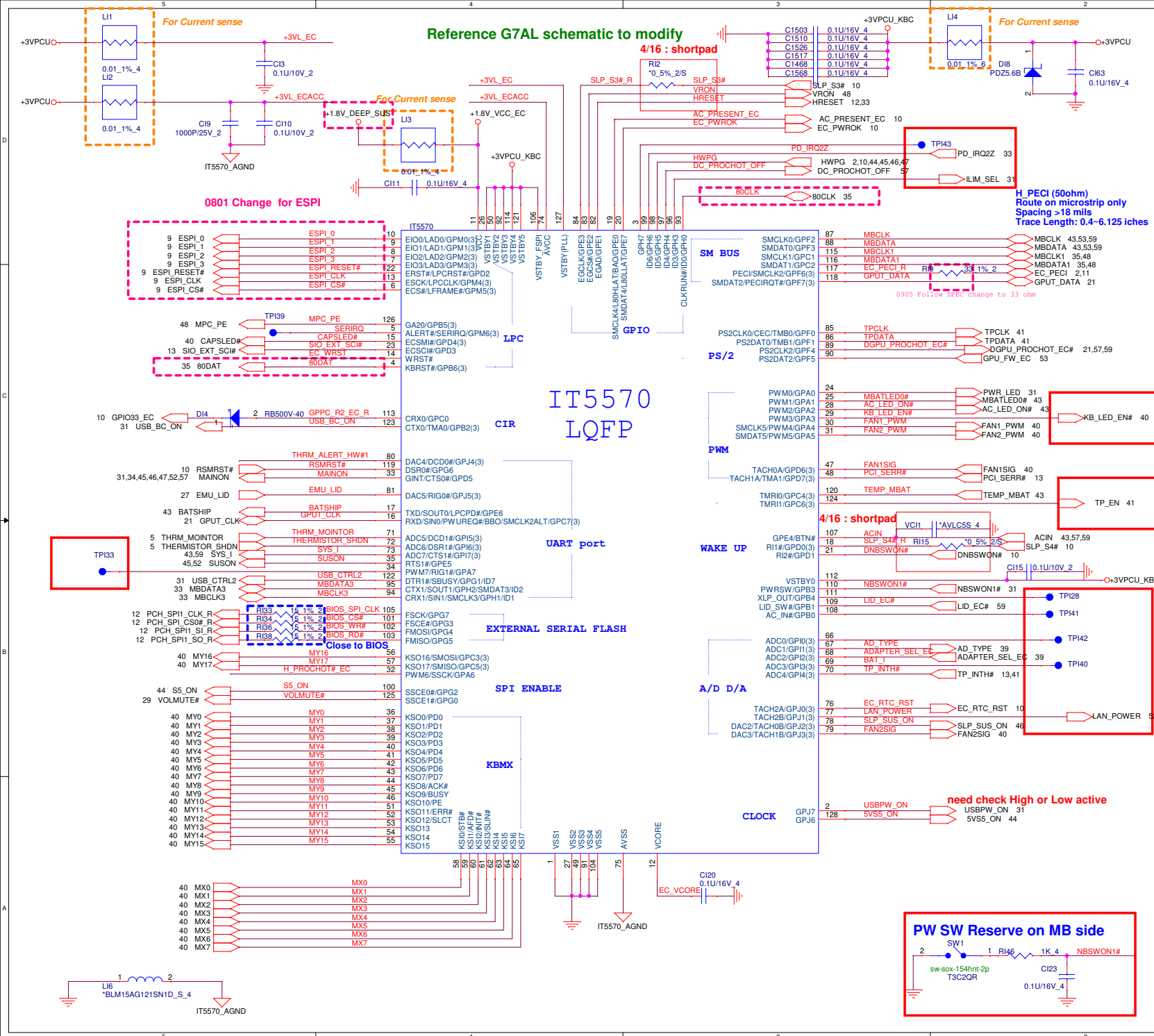


0902 Follow G3H use normal open

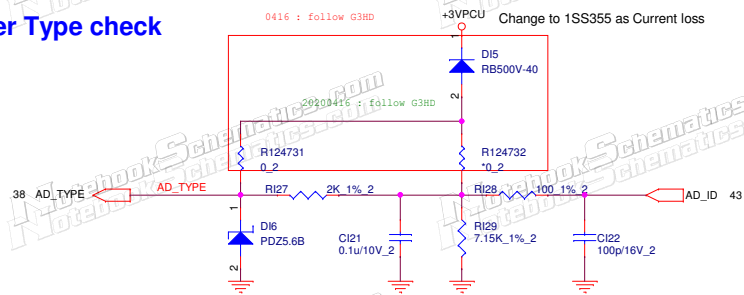


Pin Define		
Pin No.	NAME	Pin No. NAME
1	CD/DAT3	8 DAT1
2	CMD	9 DAT2
3	Vss1	10 WP Pin
4	VDD	11 CD Pin
5	CLK	
6	Vss2	
7	DAT0	

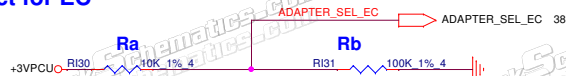




Adapter Type check



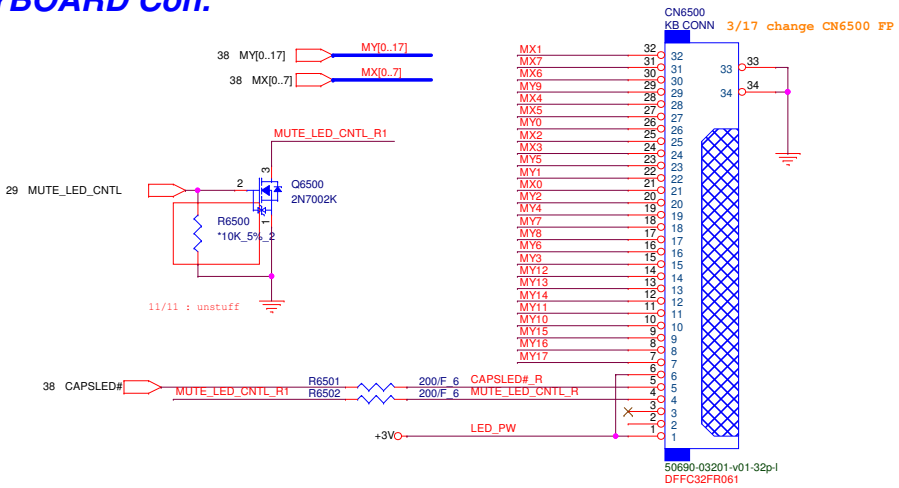
Adapter select for EC



	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	N18E
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	N18P
135W	10K(CS31002FB26)	17.8K(CS31782FB10)	2.11V	N17P
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

Adapter Type check

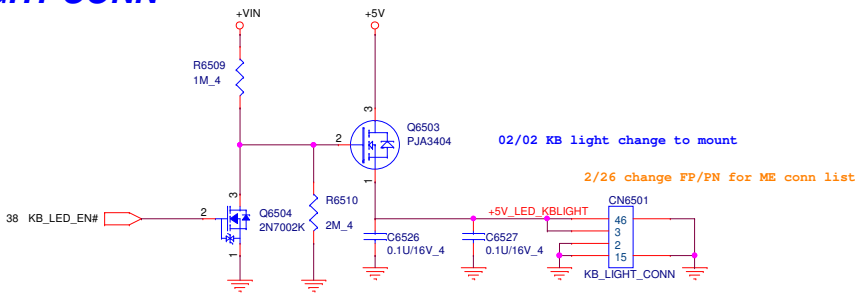
KEYBOARD Con.



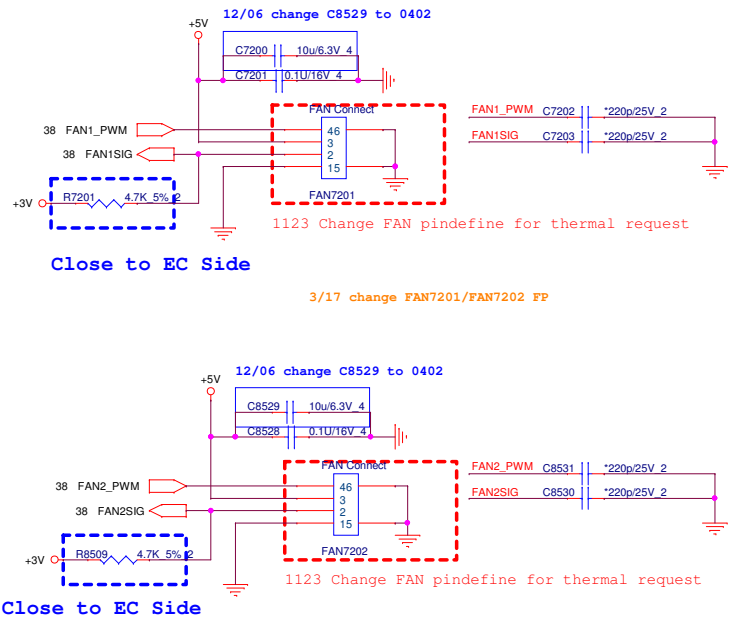
0821 follow starmade del KB PU RES

MY5	C6500	220p/25V 2
MY6	C6501	220p/25V 2
MY3	C6502	220p/25V 2
MY7	C6503	220p/25V 2
MY8	C6504	220p/25V 2
MY9	C6505	220p/25V 2
MY10	C6506	220p/25V 2
MY11	C6507	220p/25V 2
MY1	C6508	220p/25V 2
MY2	C6509	220p/25V 2
MY4	C6510	220p/25V 2
MY0	C6511	220p/25V 2
MX4	C6512	220p/25V 2
MX6	C6513	220p/25V 2
MX3	C6514	220p/25V 2
MX2	C6515	220p/25V 2
MX7	C6516	220p/25V 2
MX0	C6517	220p/25V 2
MX5	C6518	220p/25V 2
MX1	C6519	220p/25V 2
MY12	C6520	220p/25V 2
MY13	C6521	220p/25V 2
MY14	C6522	220p/25V 2
MY15	C6523	220p/25V 2
MY16	C6524	220p/25V 2
MY17	C6525	220p/25V 2

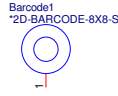
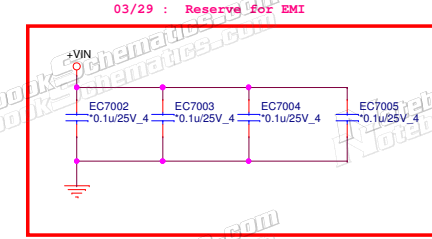
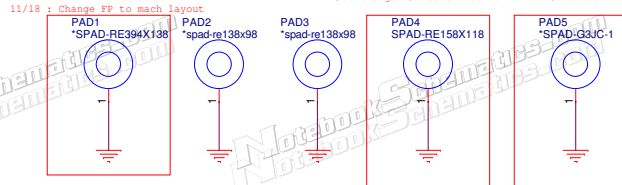
KB LIGHT CONN



FAN

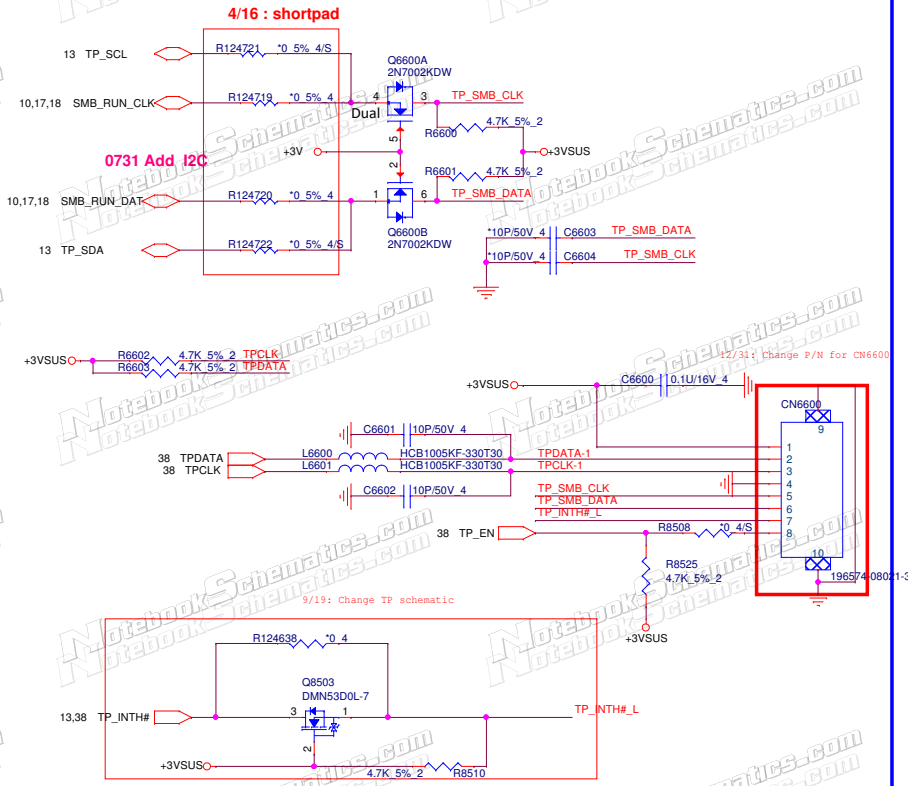


0827 DEL RGB reserved



9/19: Del Cap

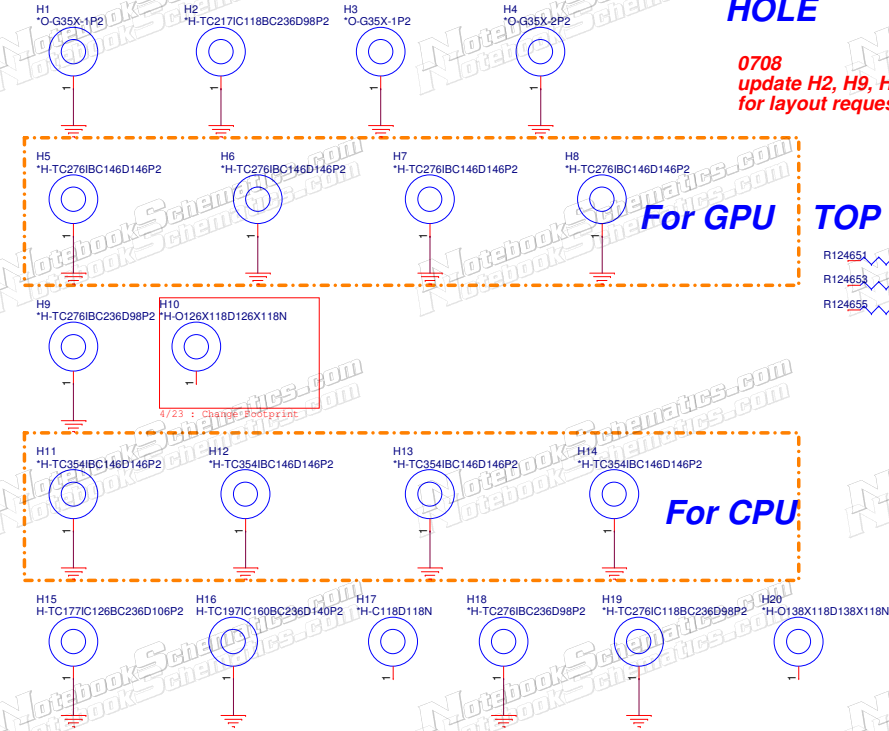
Touch Pad Connector



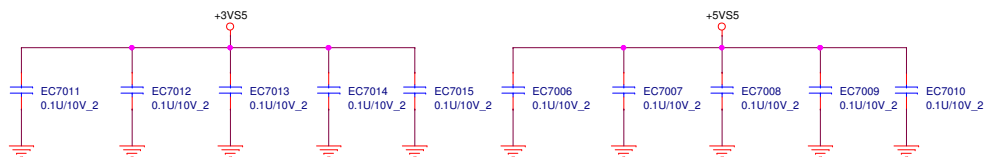
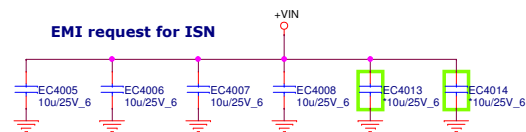
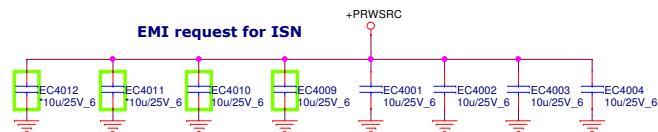
HOLE

0708
update H2, H9, H15, H16, H17, H18, H19, H20
for layout request

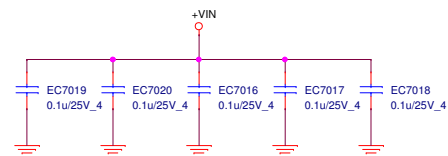
For GPU TOP for Vendor ID

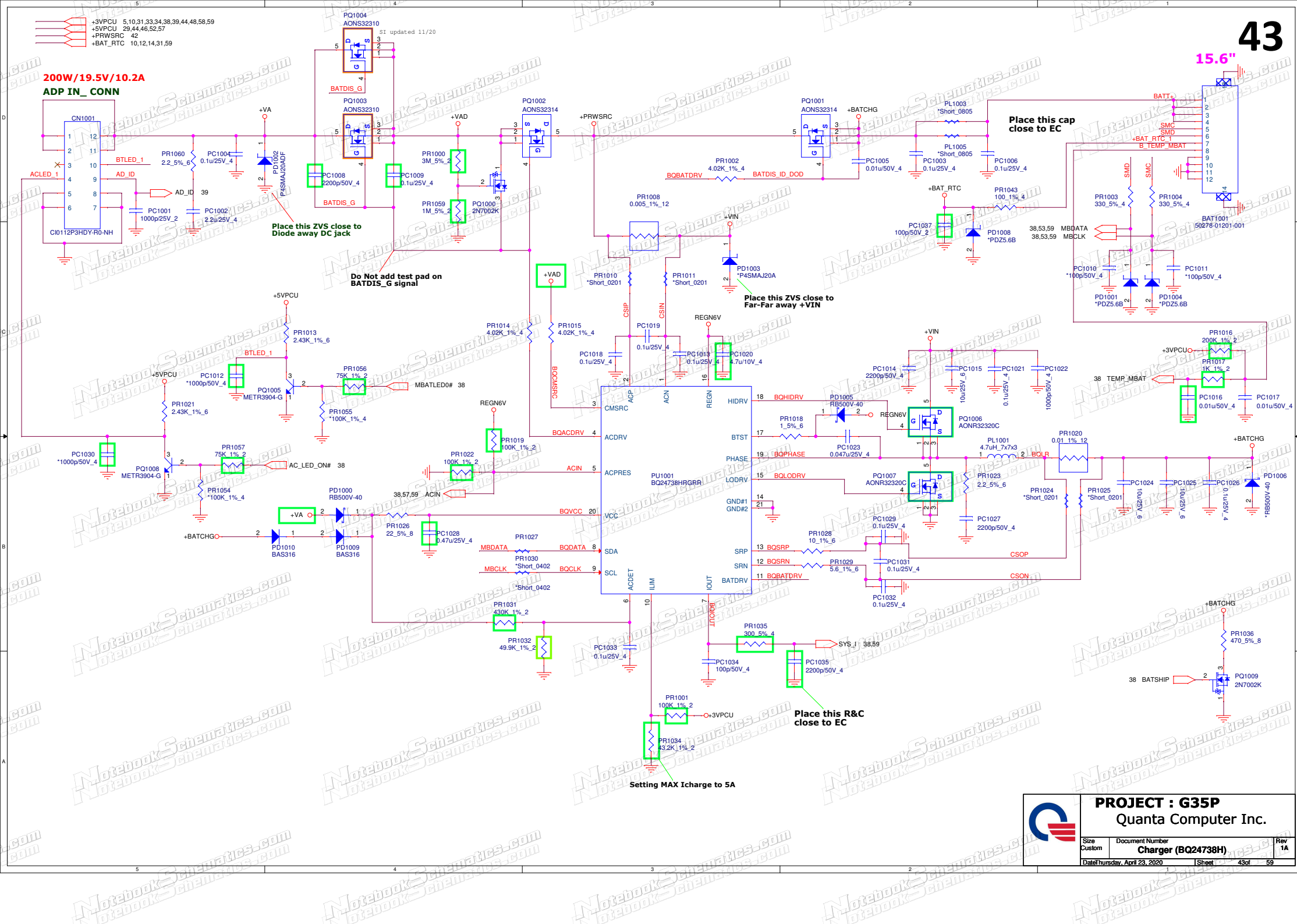


WLAN nut SSD nut



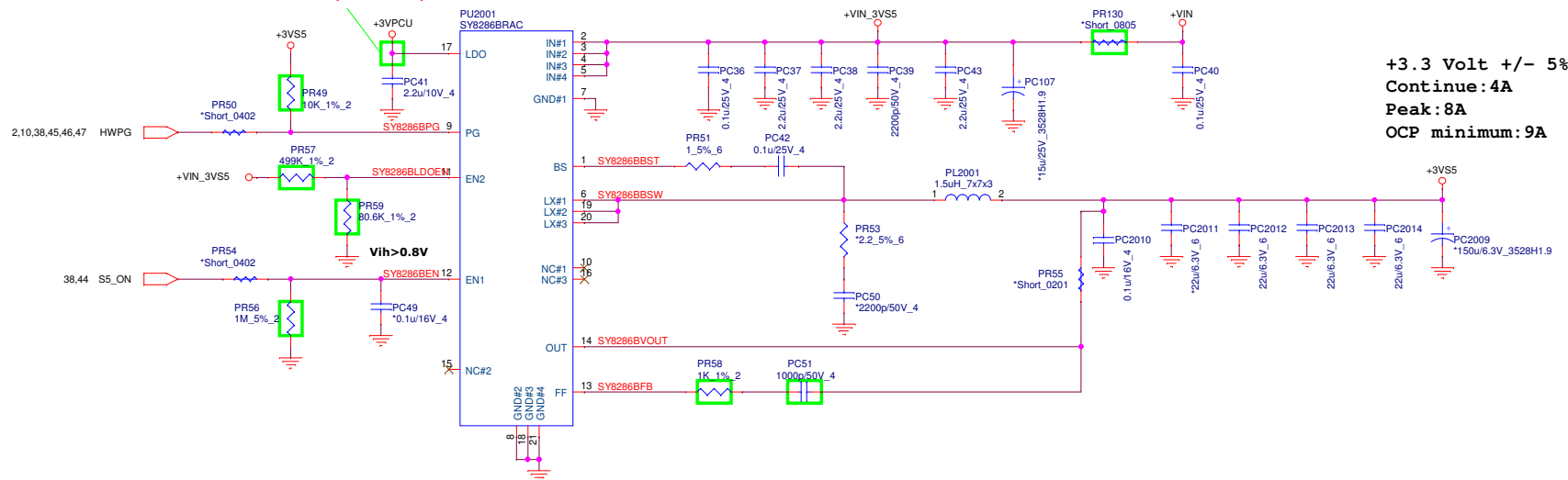
9/27 : For EMI suggest



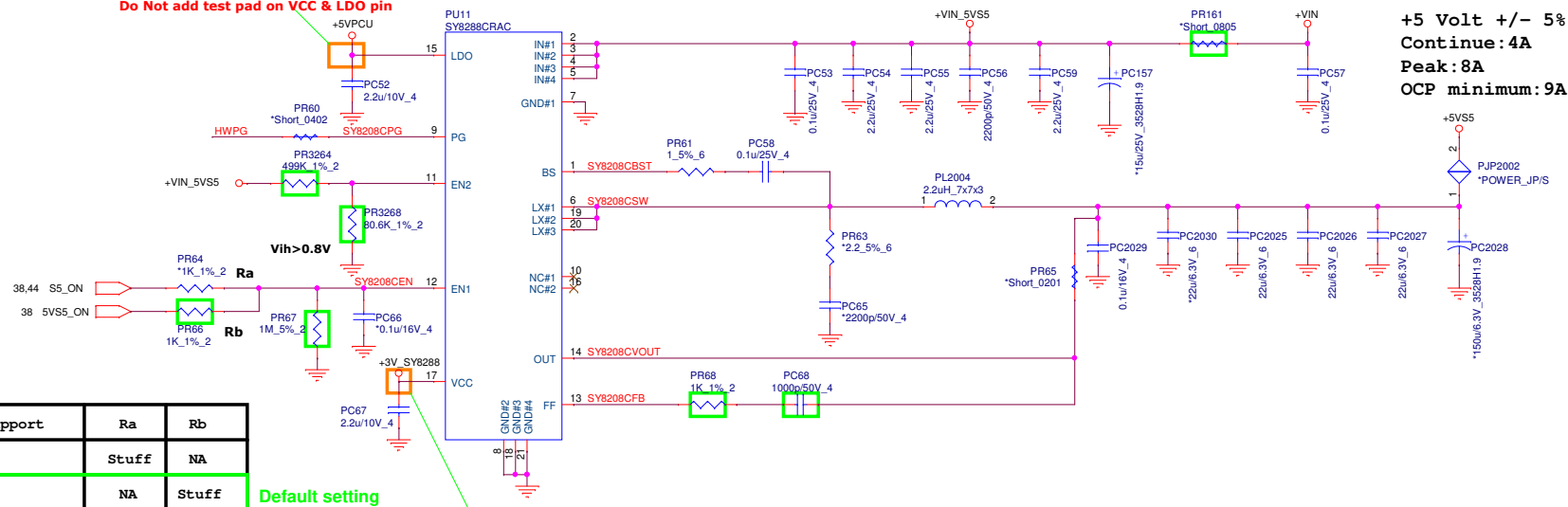


+VIN 27,40,41,42,43,45,46,47,49,51,54,56
 +3VS5 10,12,14,22,31,32,33,34,38,42,45,46,47,48,52,57,58
 +5VS5 10,31,33,42,45,46,47,52,53,56,57
 +3VPCU 5,10,31,33,34,38,39,43,48,58,59
 +5VPCU 29,43,46,52,57

Do Not add test pad on LDO pin



Do Not add test pad on VCC & LDO pin



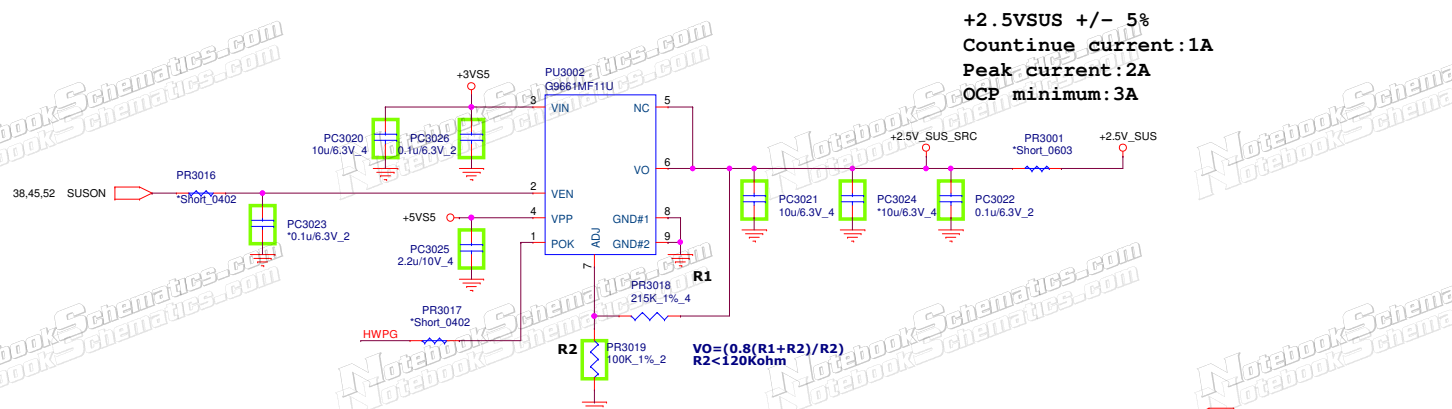
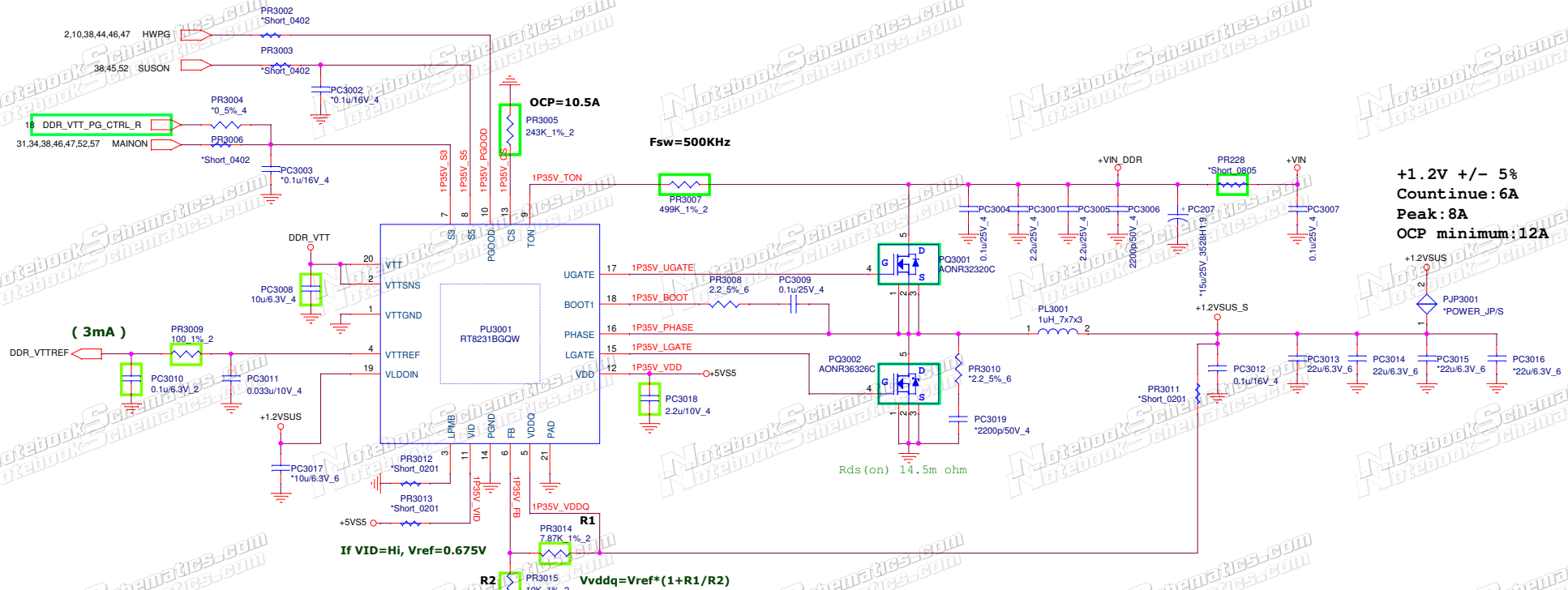
USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

Default setting


Do Not add test pad on VCC & LDO pin

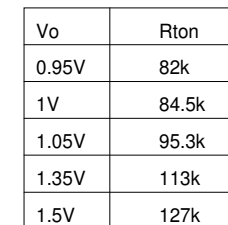
Link H/W prohot circuit

3VCC is to make use of internal driver 10mA maximum when heavy loading (internal current limit is 15mA typ.)

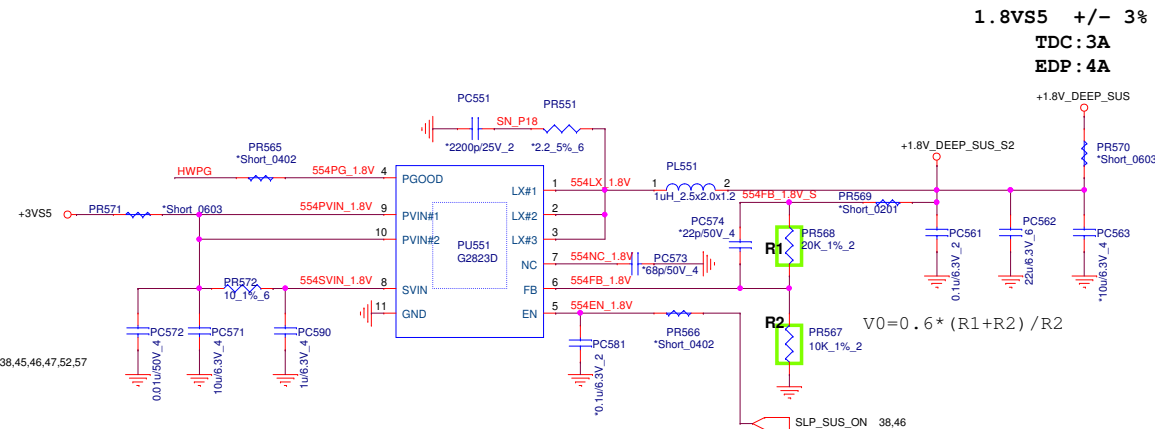
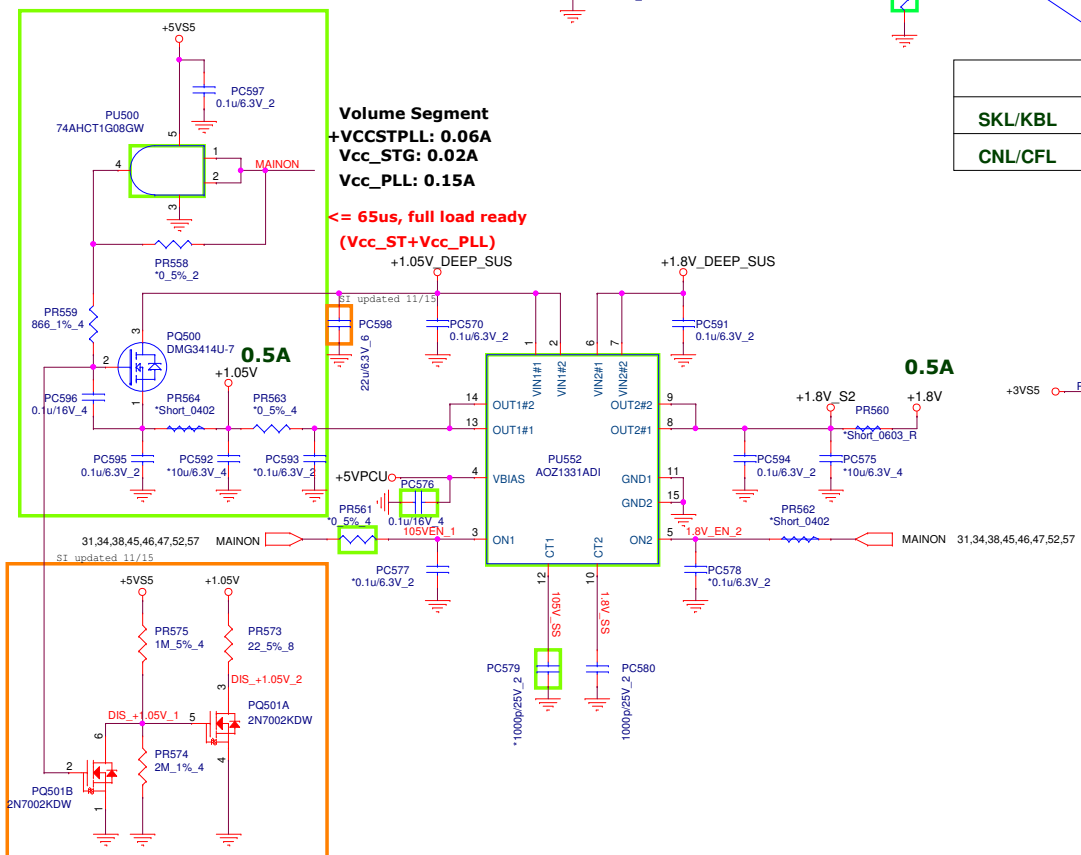


+VIN 27,40,41,42,43,44,46,47,49,51,54,56
 +5VS5 10,31,33,42,44,46,47,52,53,56,57
 +1.2VSUS 2,6,10,17,18,47
 DDR_VTT 17,18
 +2.5V_SUS 17,18

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	1.91K	CS21912FB13	0.95V
SKL/KBL		CS22612FB15	1V
CNL/CFL	3.16K	CS23162FB04	1.05V



Volume Segment

SKY/KBY-U22/U42/U23e

Vcc_IO: 3.4A/1V

Stuff PU601

Volume Segment

SKY/KBY-H 22/42/44e

Vcc_IO: 5.5A/0.95V

Stuff PU601 & merge 1V_deep_sus

Volume Segment

CNL U22

Vcc_IO: 5.1A/0.95V

Vcc_IO: Can merge +1.05V_deep_sus

Unstuff PU603

Unstuff PU601

Default setting

Volume Segment

CFL H6/H4

Vcc_IO: 6.4A/0.95V

Stuff PU603

Unstuff PU601

C10: turn off VCCPLL_OC, VCCIO, VCCSTG

Unstuff PU601=G5027

For C10 Add

CFL=0.95V/LPM=0V
+VCC_IO +/-5%
Continuous current: A
Peak current: 6.4A

<= 240us, full load ready
TDC:0.26A

VID0_VCCIO	VID1_VCCIO	LP#	VCCIO
X	X	0	0V
0	0	1	0.85V
1	0	1	0.875V
0	1 (IC internal PU High)	1	0.95V

Default setting

+3V_DEEP_SUS 9,10,12,13,14,16,18,34
+VCCSTG 2,6,38
+3VS5 10,12,14,22,31,32,33,34,38,42,44,45,46,48,52,57,58
+5VS5 10,31,33,42,44,45,46,52,53,55,57
+VCCIO 3,6
+1.05V_DEEP_SUS 10,14,46
+1.2V_VCCPLL_OC 6
+1.2VSUS 2,6,10,17,18,45
+VIN 27,40,41,42,43,44,45,46,49,51,54,56

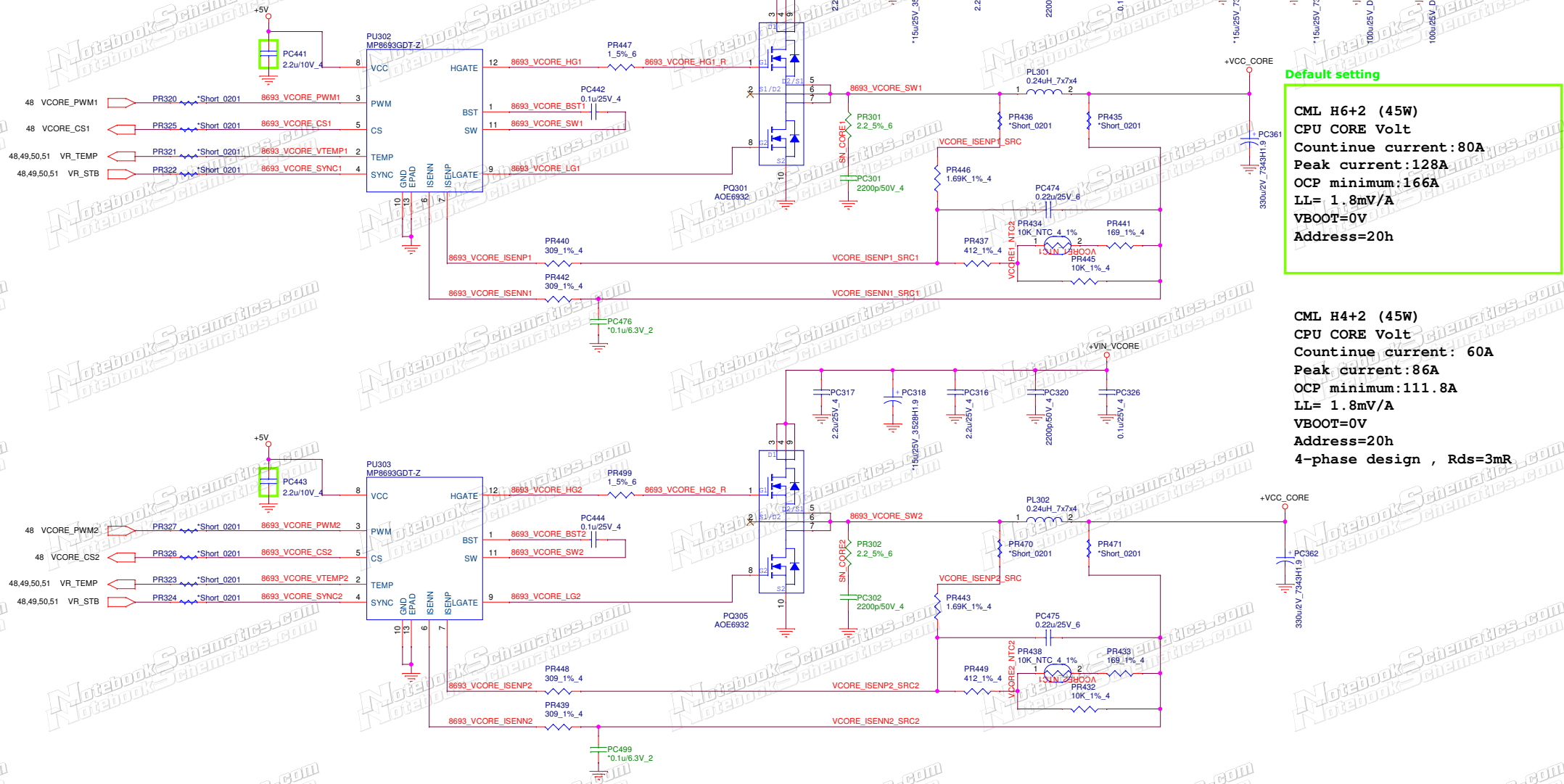


PROJECT : G35P

Quanta Computer Inc.

Size Custom Document Number
+1.0V/+VCCSTPLL/+VCCIO
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+VIN_VCORE 48,50,51
+5VS5 10,31,33,42,44,45,46,47,52,53,56,57
+VCC_CORE 7,48,50
+VIN 27,40,41,42,43,44,45,46,47,51,54,56



Default setting

CML H6+2 (45W)
CPU CORE Volt
Continue current: 80A
Peak current: 128A
OCP minimum: 166A
LL= 1.8mV/A
VBOOT=0V
Address=20h

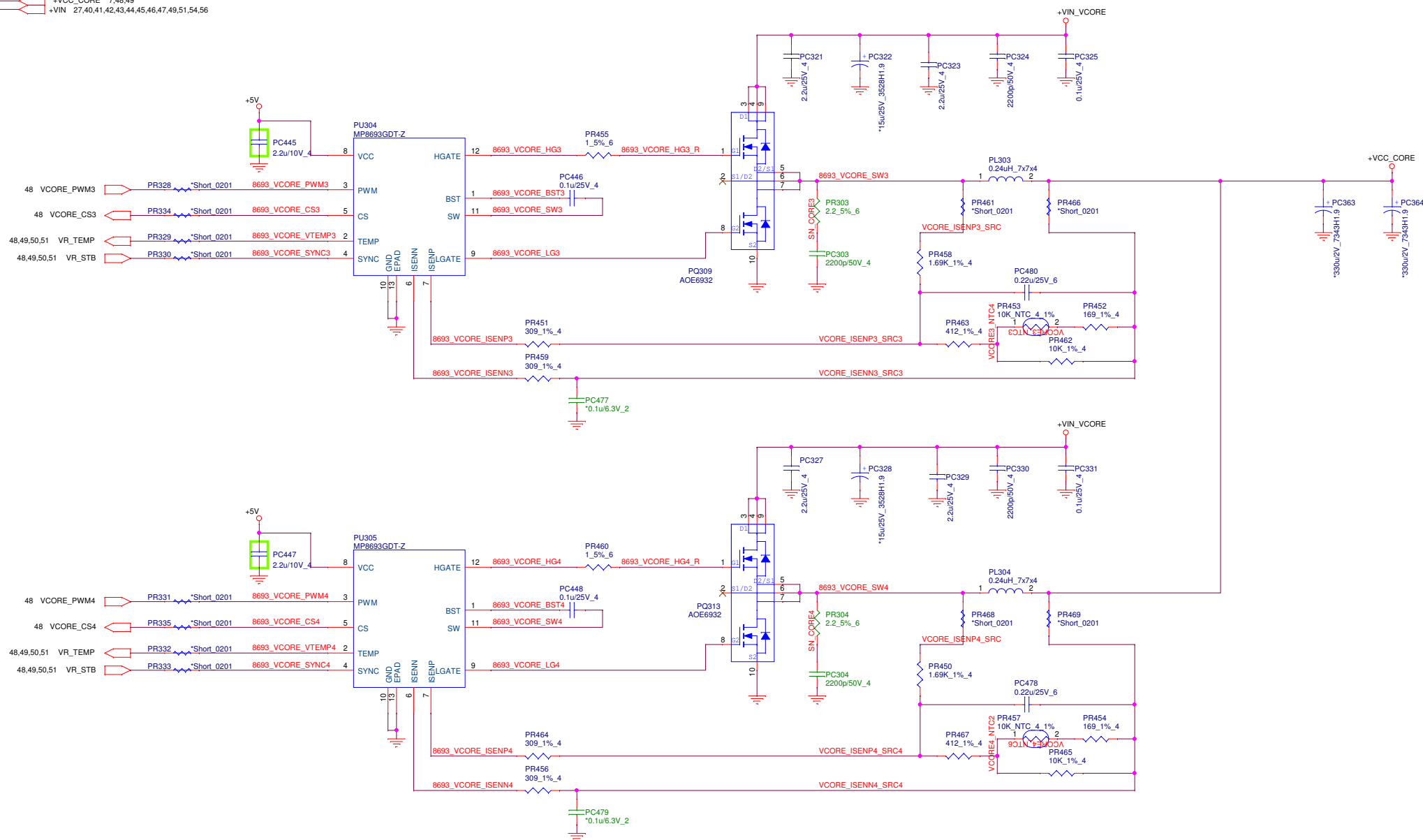
CML H4+2 (45W)
CPU CORE Volt
Continue current: 60A
Peak current: 86A
OCP minimum: 111.8A
LL= 1.8mV/A
VBOOT=0V
Address=20h
4-phase design, Rds=3mR

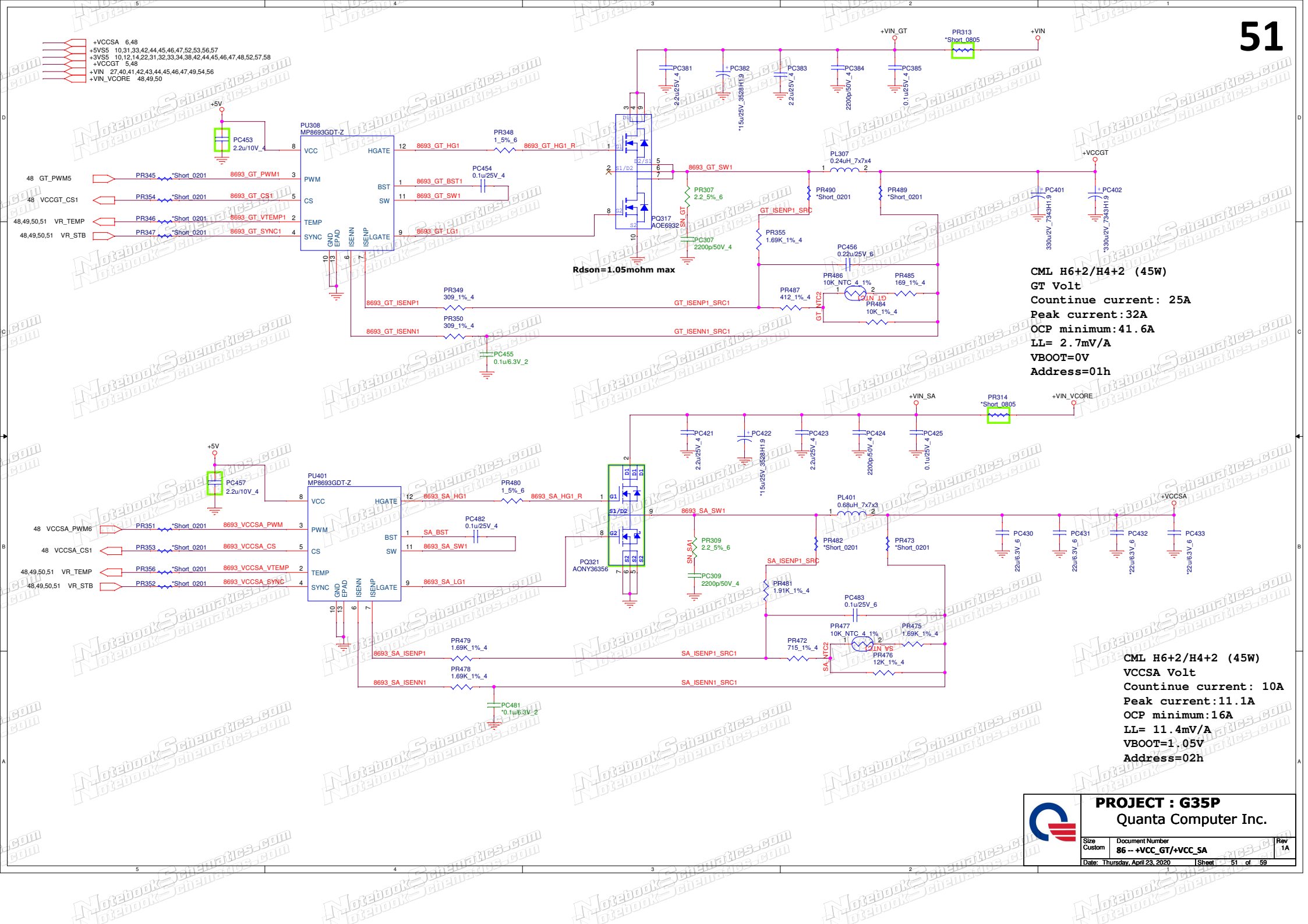
ALL POWER CLIP		Cout
CFL H6+2	4 phase BAM69320002 ; AOE6932 ; 1.8mR	2PCS 330u/7343
CFL H4+2	4 phase BAM69360000 ; AOE6936 ; 3mR	2PCS 330u/7343

Default setting

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Custom	85 - +VCC_CORE (MP86903-C)	1A	
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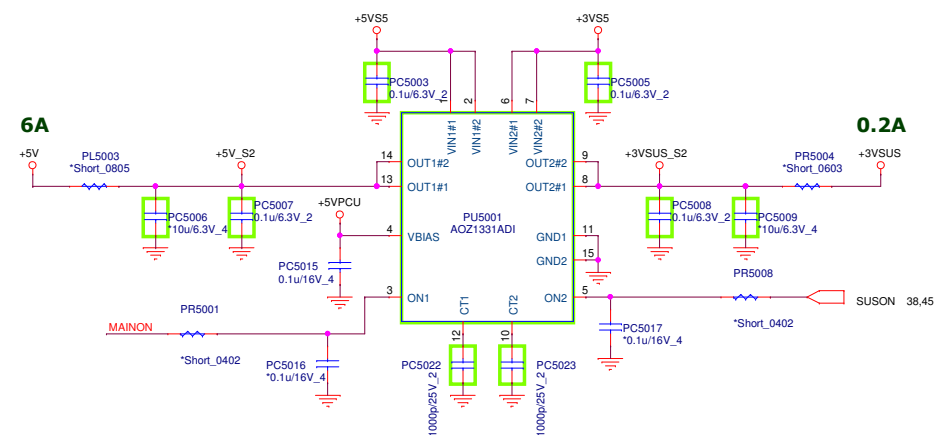
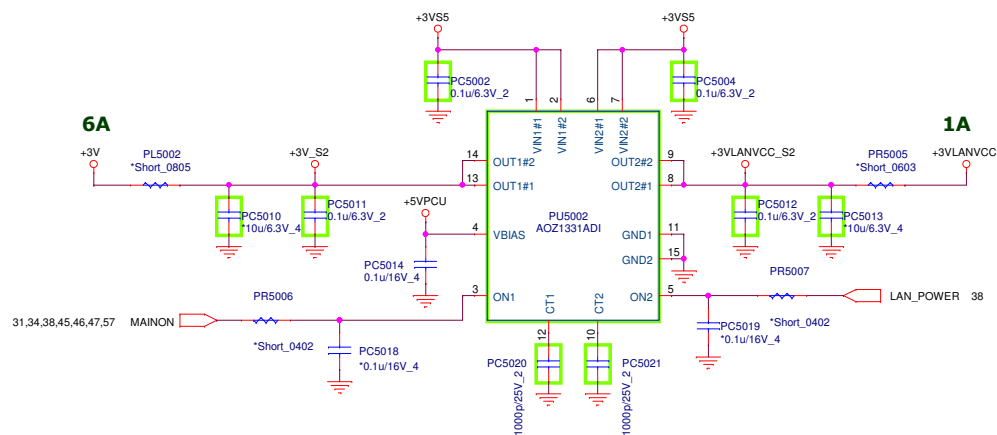
+VIN_VCORE 48,49,51
 +5VS5 10,31,33,42,44,45,46,47,52,53,56,57
 +VCC_CORE 7,48,49
 +VIN 27,40,41,42,43,44,45,46,47,49,51,54,56

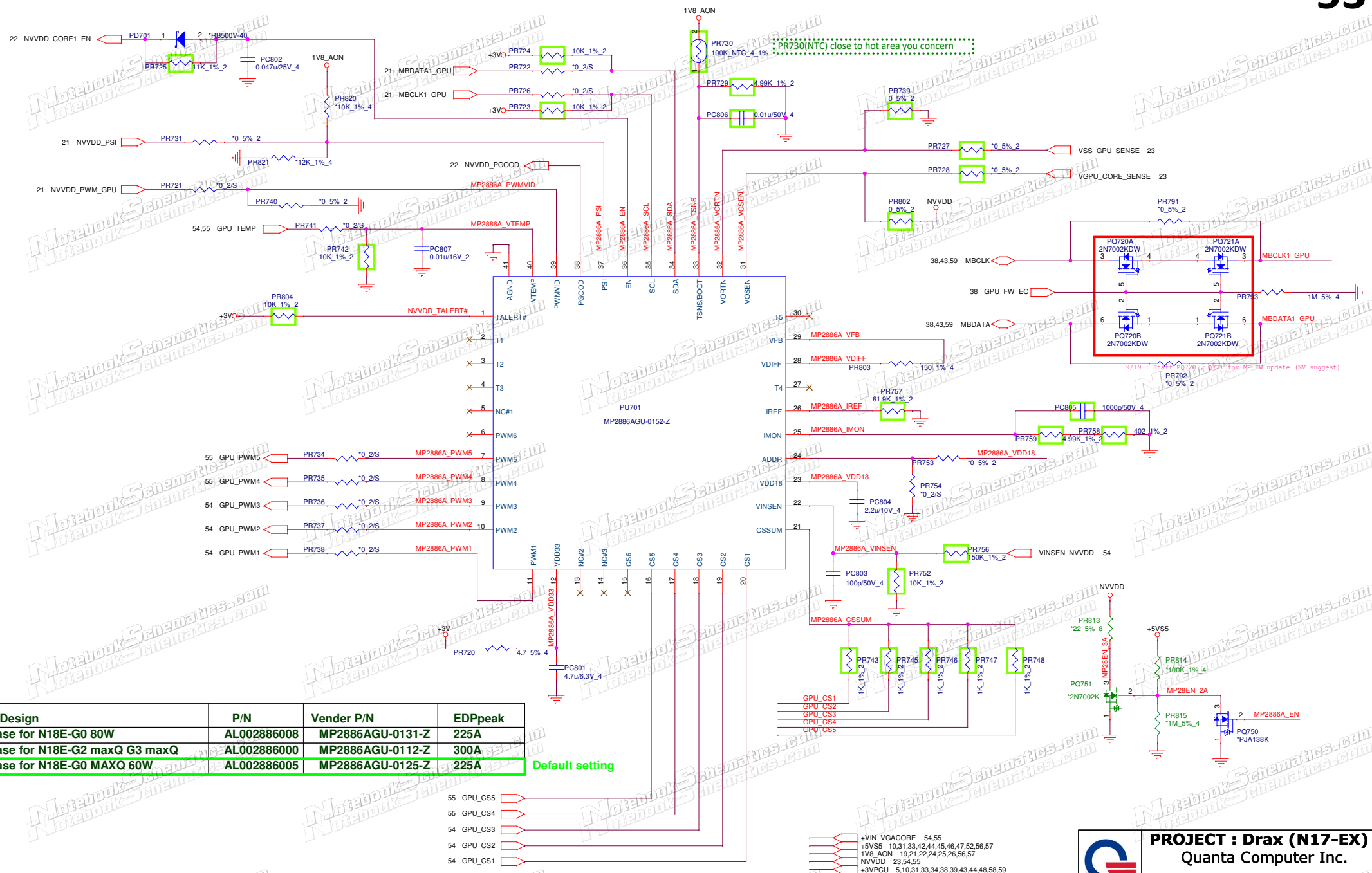




```
CML H6+2/H4+2 (45W)
VCCSA Volt
Countinue current: 10A
Peak current:11.1A
OCP minimum:16A
LL= 11.4mV/A
VBOOT=1.05V
Address=02h
```

+3V 9,10,11,13,16,17,18,21,27,29,32,34,35,36,37,38,40,41,48,53,54,55,56,57
 +5V 27,28,29,32,35,40,49,50,51,58
 +3VS5 10,12,14,22,31,32,33,34,38,42,44,45,46,47,48,57,58
 +5VS5 10,31,33,42,44,45,46,47,53,56,57
 +3VSUS 41
 +3VLAVCC 36
 +3V_DEEP_SUS 9,10,12,13,14,16,18,34,47



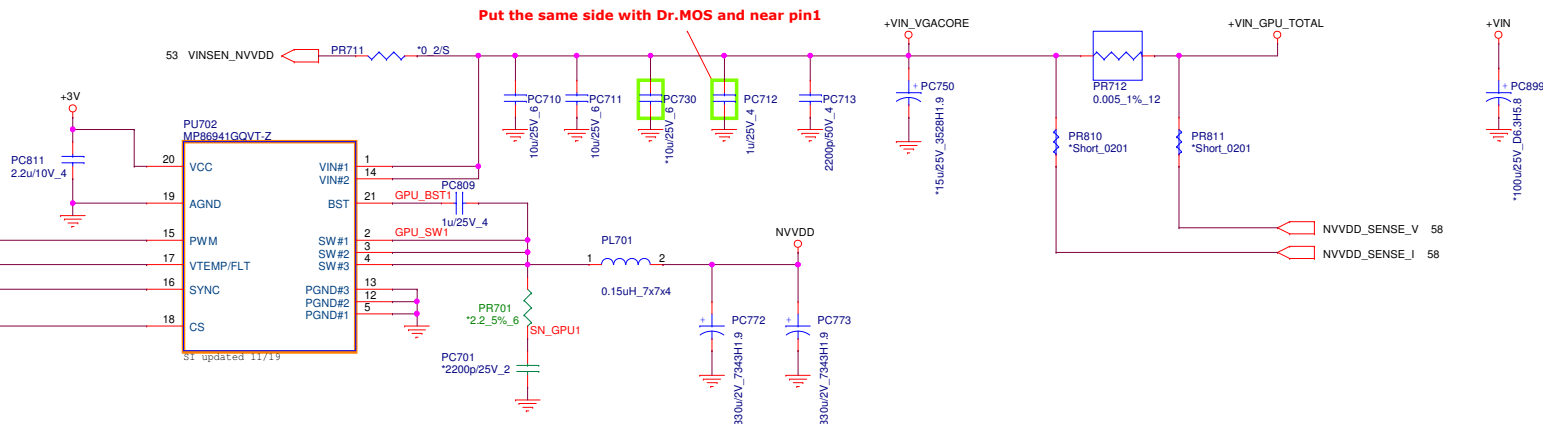


+VIN_GPU_TOTAL 56
+5VS5 10,31,33,42,44,45,46,47,52,53,56,57
NVVDD 23,53,55
+VIN_VGACORE 55

MOS Temperature

53 GPU_PWM1
53,54,55 GPU_TEMP

53 GPU_CS1



Put the same side with Dr.MOS and near pin1

+VIN_VGACORE

+VIN_GPU_TOTAL

+VIN

N18E G0 MaxQ TGP 60W Boost 70W
TGP : 60W Model+5W Mode2+10W
TDP : Model:45W Mode2:50W
GPU CORE Volt
Cuntinue current: 51A
Model 57A Mode2 63A
Peak current: 225A/6uSec.
OCP Minimum: 240A.
LL=
VBOOT=0.8V
Eff > 86%
DC < +/- 20mV
Setting time <100uS

Put the same side with Dr.MOS and near pin1

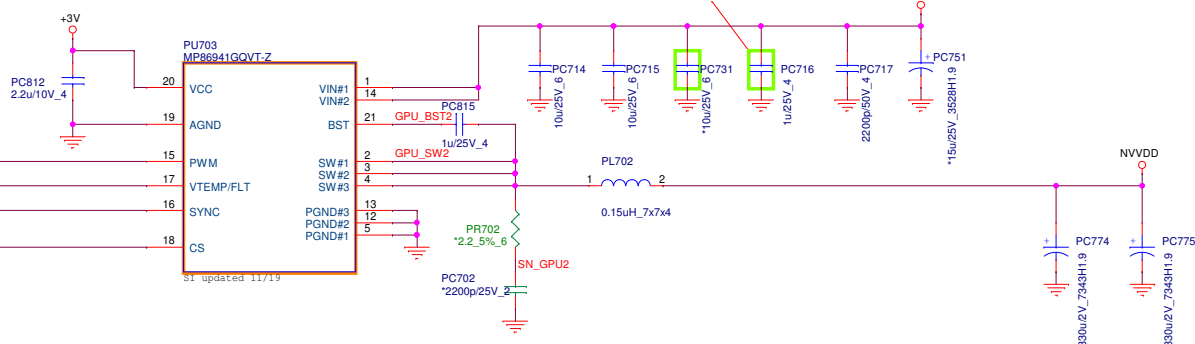
+VIN_VGACORE

NVVDD

53 GPU_PWM2

53,54,55 GPU_TEMP

53 GPU_CS2



Put the same side with Dr.MOS and near pin1

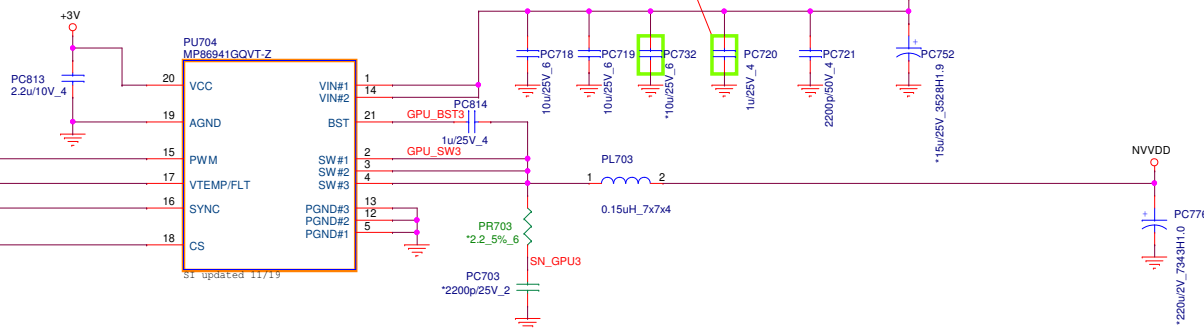
+VIN_VGACORE


NVVDD

53 GPU_PWM3

53,54,55 GPU_TEMP

53 GPU_CS3

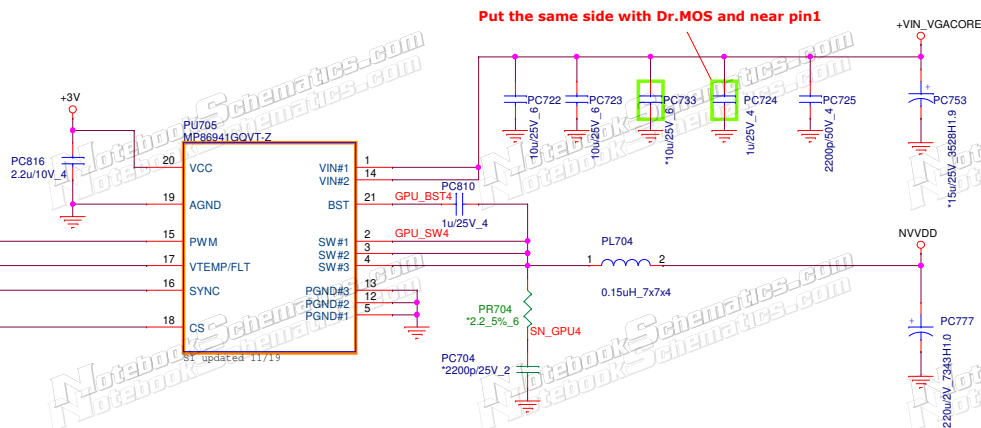



	PROJECT : Drax (N17-EX)		
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+5VS5 10,31,33,42,44,45,46,47,52,53,56,57
NVVDD 23,53,54
+VIN_VGACORE 54


MOS Temperature


53 GPU_PWM4 →
53,54,55 GPU_TEMP ←
+3V
53 GPU_CS4 ←

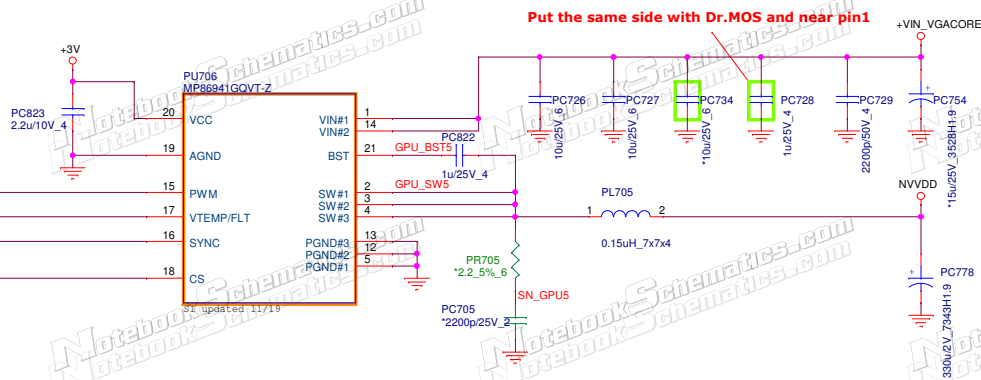


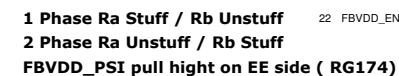
53 GPU_PWM5 

53.54.55 GPU_TEMP 

+3V 

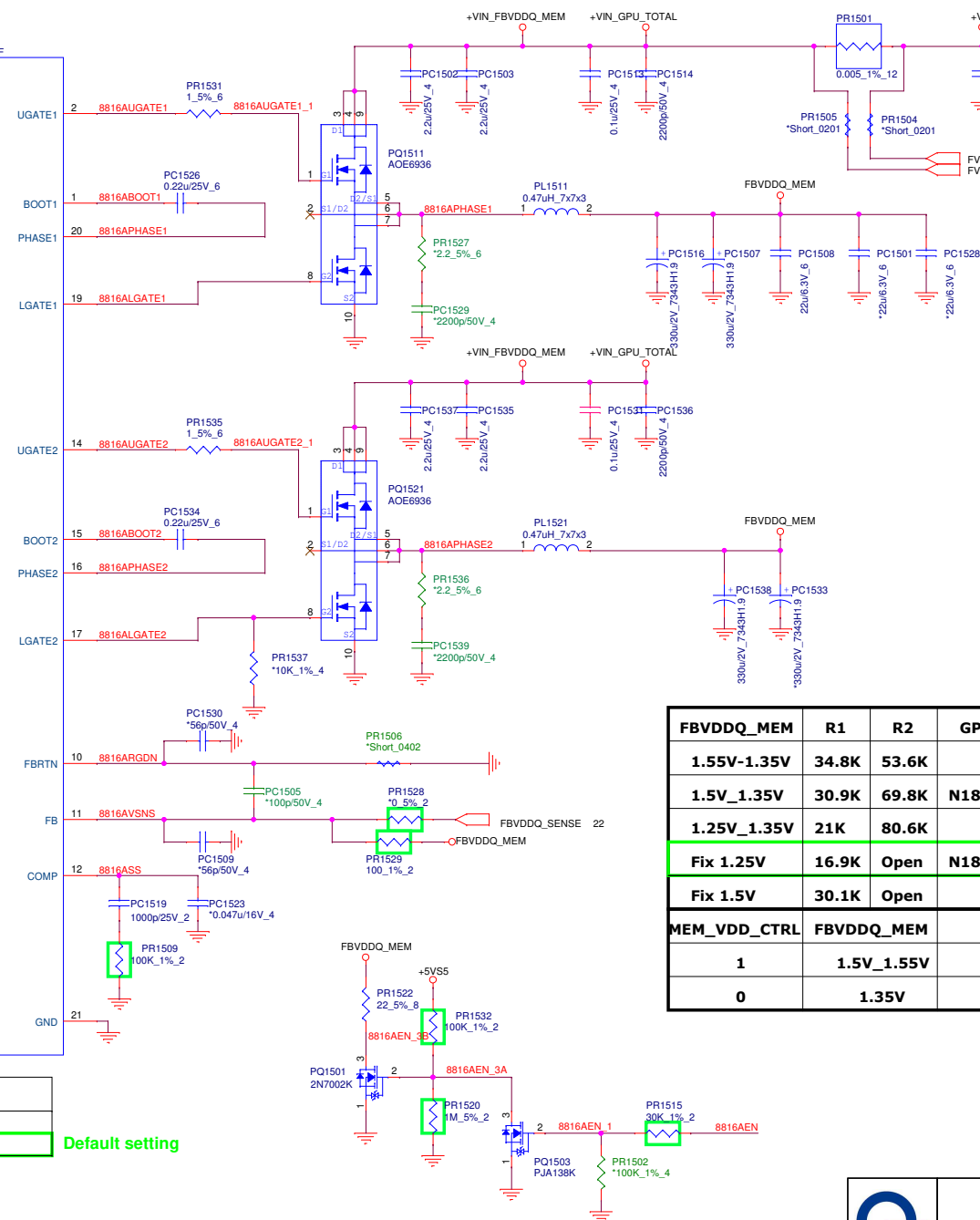
53 GPU_CS5 





	Ra	Re	Rf	OCF
N18P G0 1-Phase	Stuff	46.4K	86.6K	25A
N18E G0 2-Phase	Unstuff	47.5K	78.7K	48A

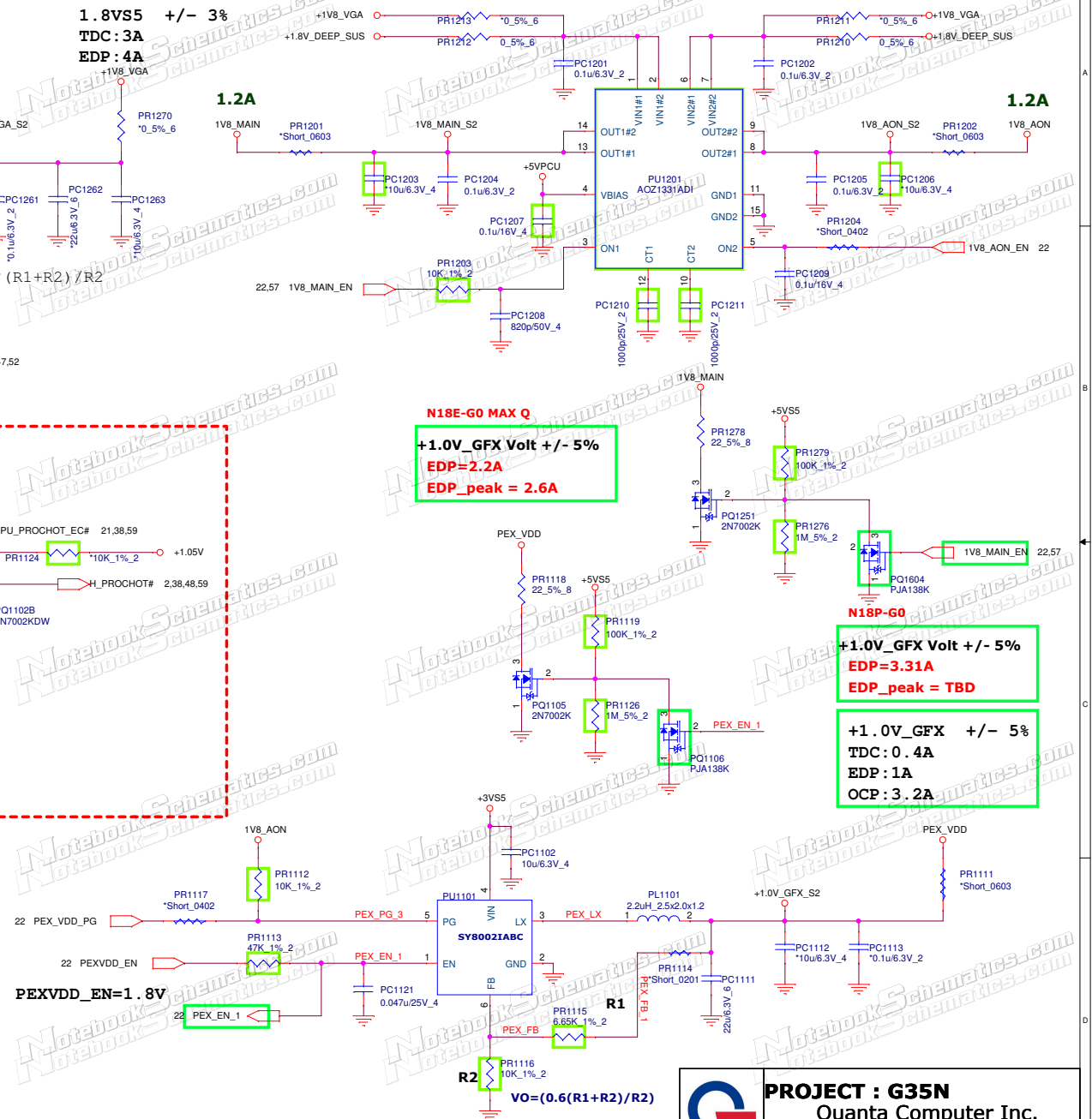
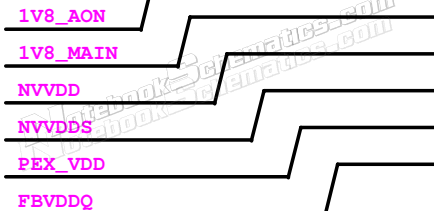
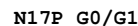
Default setting



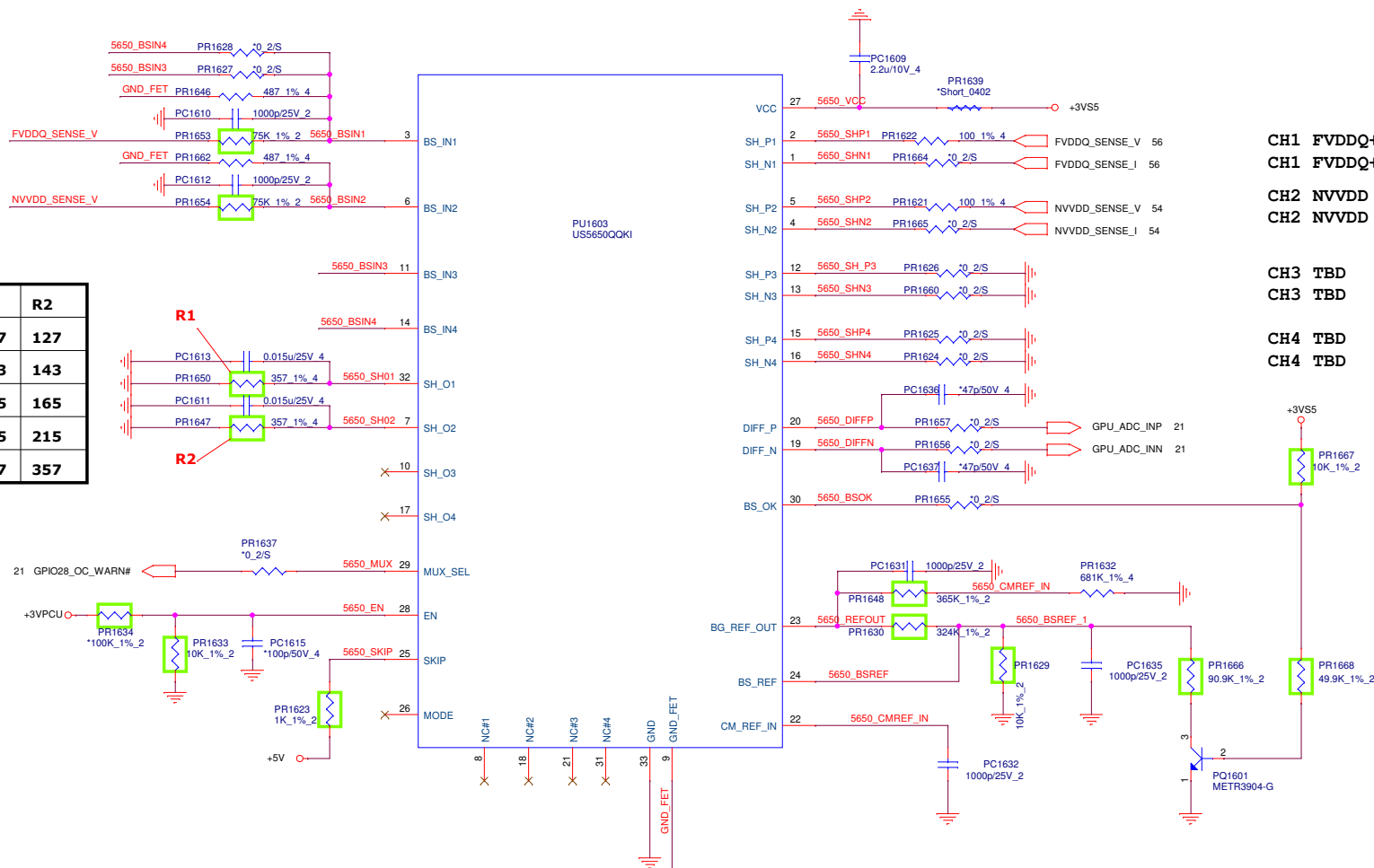
N18E-GO MAX Q(TGP 60W)
FBVDDQ_MEM=1.5V
EDP-C: 30A
EDP-P: 40A
OCV minimum: 48A
LL=0m V/A

FBVDDQ_MEM	R1	R2	GPU Type
1.55V-1.35V	34.8K	53.6K	
1.5V_1.35V	30.9K	69.8K	N18P
1.25V_1.35V	21K	80.6K	
Fix 1.25V	16.9K	Open	N18E-G0 MAX-Q
Fix 1.5V	30.1K	Open	
MEM_VDD_CTRL	FBVDDQ_MEM		
1	1.5V_1.55V		
0	1.35V		

Default setting



UPI OVR Setting	R1	R2
150W+	127	127
115W to 130W	143	143
100W to 110W	165	165
75W to 90W	215	215
70W or Lower	357	357



CH1 FVDDQ+NVDD VOLTAGE
CH1 FVDDQ+NVDD CURRENT

CH2 NVDD VOLTAGE
CH2 NVDD CURRENT

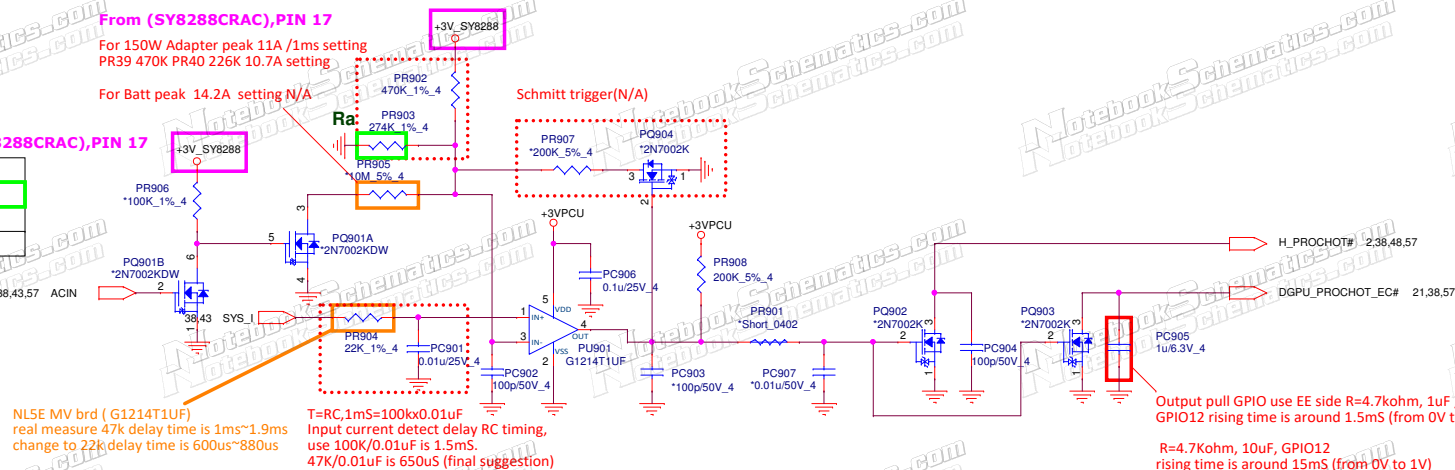
CH3 TBD
CH3 TBD

CH4 TBD
CH4 TBD



Adapter	Peak Current	Ra
200W	12.3A (300mS)	274K
150W	10A (300mS)	205K
135W	10A (100mS)	205K

From (SY8288CRAC),PIN 17



Output pull GPIO use EE side $R=4.7\text{kohm}$, $1\mu\text{F}$,
GPIO12 rising time is around 1.5mS (from 0V to 1V)

R=4.7Kohm, 10uF, GPIO12
rising time is around 15mS (from 0V to 1V)

R=47Kohm. 1uF. >> suppose is same as above 15mS final selection.
(If need more time delay, could consider change R or C value)



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